

For the "loose" diagram seen in Fig.1

Follow the method of partition to reduce the number of states. Show ALL your steps explicitly.

(15 pts.)

b. Draw the reduced flow chart

(5 pts.)

Fig. 2 shows a flow chart and a state assignment map next to it. Show explicitly whether or not EACH of the rules is obeyed: Rule 0 (6pts.), Rule 1 (6pts.), Rule 2 (6pts.), and Rule 3 (2pts.).

(20 pts.)

For a "One Hot" method to implement the ASM seen in Fig.2. ?

a. Prepare the appropriate table.

(10 pts.)

b. Draw the circuit for D flip-flops

(10 pts.)

Answer 6 of the following 7 questions:

(6x7 = 42 pts.)

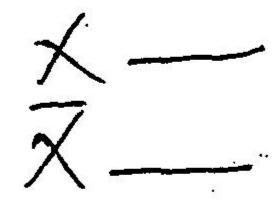
- a. Find the cycle(s) for the wrongly wired "Shift Counter" in Fig.3
- b. Prepare the Excitation Table of the flip-flop seen in Fig.4, and Identify its type. (D, JK, SR, T, etc.)
- -Identify the gadgets seen in Fig.5. Say which is useful for FET and which RET
- Describe the "Luxury Implementation" of ASM's with the aid of a diagram.



- Why do we always see an OR gate at the input of the flip-flops in a counter?
- Calculate explicitly the total number of possible state assignments for the ASM of Fig.2?
- Prove that the number of unique assignments for an ASM of three states is three.

Good Luck!

3x20 + 42 = 102



Bonus: Find the short cycle for a shift counter composed of 6 flip-flops.

Note: Bonus RULE ZERO applies.

