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EECE 320 – Digital Systems Design

Homework 3

Problem 1 [10 pts]: A 4-bit "comparator" circuit receives two 4-bit unsigned numbers $\mathbf{P=P_3P_2P_1P_0}$ and $\mathbf{Q=Q_3Q_2Q_1Q_0}$. Design a minimal sum-of-products circuit that produces a 1 output if and only if $\mathbf{P < Q}$. Modify your design to work with 2's complete numbers.

Problem 2 [10 pts]: Prove whether or not the following expression is a minimal sum. Do it *without* using K-maps.

$$\mathbf{F = S'.T.U.V.W + S'.T.U'W.Y + S'.T.V.W.X'.Y}$$

Problem 3 [14 pts]: Consider the following functions $\mathbf{F_1 = A'B'C'D' + A'C'D + BC'D' + ABD + AB'C'}$ and $\mathbf{F_2 = \Sigma_{W,X,Y,Z}(4,5,9,13,15) + d(0,1,7,11,12)}$. Determine the following for each of $\mathbf{F_1}$ and $\mathbf{F_2}$: (a) Canonical SOP, (b) Canonical POS, (c) Complete SOP, (d) Complete POS, (e) Minimal SOP, (f) Minimal POS (g) Essential prime-implicants.

Problem 4 [20 pts]: Find the minimal SOP and minimal POS for each of the following 5-variable functions:
(a) $\mathbf{F_1 = \Sigma_{V,W,X,Y,Z}(5,7,13,15,16,20,25,27,29,31)}$, (b) $\mathbf{F_2 = \Sigma_{V,W,X,Y,Z}(0,7,8,9,12,13,15,16,22,23,30,31)}$, (c) $\mathbf{F_3 = \Pi_{V,W,X,Y,Z}(4,5,10,12,13,16,17,21,25,26,27,29)}$, (d) $\mathbf{F_4 = \Sigma_{V,W,X,Y,Z}(4,6,7,9,11,12,13,14,15,20,22,25,27,28,30) + d(1,5,29,31)}$.

Problem 5 [10 pts]: Find the minimal-output sum-of-products expressions for $\mathbf{F = \Sigma_{X,Y,Z}(0,1,2)}$, $\mathbf{G = \Sigma_{X,Y,Z}(1,4,6)}$, and $\mathbf{H = \Sigma_{X,Y,Z}(0,1,2,4,6)}$. Draw the corresponding minimal logic circuit.

Problem 6 [20 pts]: For each of the following logic expressions, find all of the static hazards in the corresponding two-level AND-OR and OR-AND circuit, and then design a hazard-free circuit that realizes the same logic function: (a) $\mathbf{F_1 = WY + W'Z' + XY'Z}$, (b) $\mathbf{F_2 = W'X' + Y'Z + W'XYZ + WXYZ'}$, (c) $\mathbf{F_3 = (W+Y'+Z')(W'+X'+Z')(X'+Y+Z)}$, and (d) $\mathbf{F_4 = (W+Y+Z')(W+X'+Y+Z)(X'+Y')(X+Z)}$.

Problem 7 [20 pts]: Find the minimal SOP for the following 6-variable function:

$$\mathbf{F = \Sigma_{U,V,W,X,Y,Z}(2,4,5,6,12,13,14,15,16,17,18,19,20,21,28,29,30,31,34,38,50,51,60,61,62,63)}$$

Problem 8 [10 pts]: Design a 4-bit adder logic circuit. First design a logic circuit that adds two bits $\mathbf{A_0}$ and $\mathbf{B_0}$ and a carry in $\mathbf{C_{in0}}$, and generates a sum bit $\mathbf{S_0}$ and an output carry bit $\mathbf{C_{out0}}$. Write the minimized Boolean equations of this block. Then use this block to design a circuit that adds $\mathbf{A_3A_2A_1A_0}$ and $\mathbf{B_3B_2B_1B_0}$. Show all your connections.

Problem 9 [10 pts]: Repeat the previous problem, but now for a circuit that *subtracts* two numbers $\mathbf{A_3A_2A_1A_0}$ and $\mathbf{B_3B_2B_1B_0}$. **Hint: Use the relationship between addition and subtraction in 2's complement.**

Problem 10 [10 pts]: Design a circuit that increments a 4-bit number $\mathbf{A_3A_2A_1A_0}$ by 1. Write logic expressions for all outputs, and simplify them as much as you can. Start by designing a 1-bit incrementor circuit using its truth table.