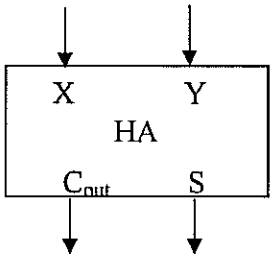
Solution

American University of Beirut
Department of Electrical and Computer Engineering

EECE 320 – Digital Systems Design
Test 3 14-11-2011

A Half adder (HA) is a combinational circuit that adds two bits and generates a Sum bit and a Carry out bit.



1. Draw the truth table of this circuit, and derive minimal algebraic expressions for S and C_{out}.

X	Y	Cout	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$C_{out} = XY$

$S = XY' + X'Y$

2. Write the VHDL code to define the entity HA.

```
entity HA is
    port (X, Y : in std_logic;
          S, Cout : out std_logic);
```

3. Write the **Dataflow** architectural description for this entity.

```
architecture dataflow of HA is
begin
    Cout <= X and Y;
    S <= (X and (Not Y)) OR ((Not X) AND Y);

end dataflow ;
```