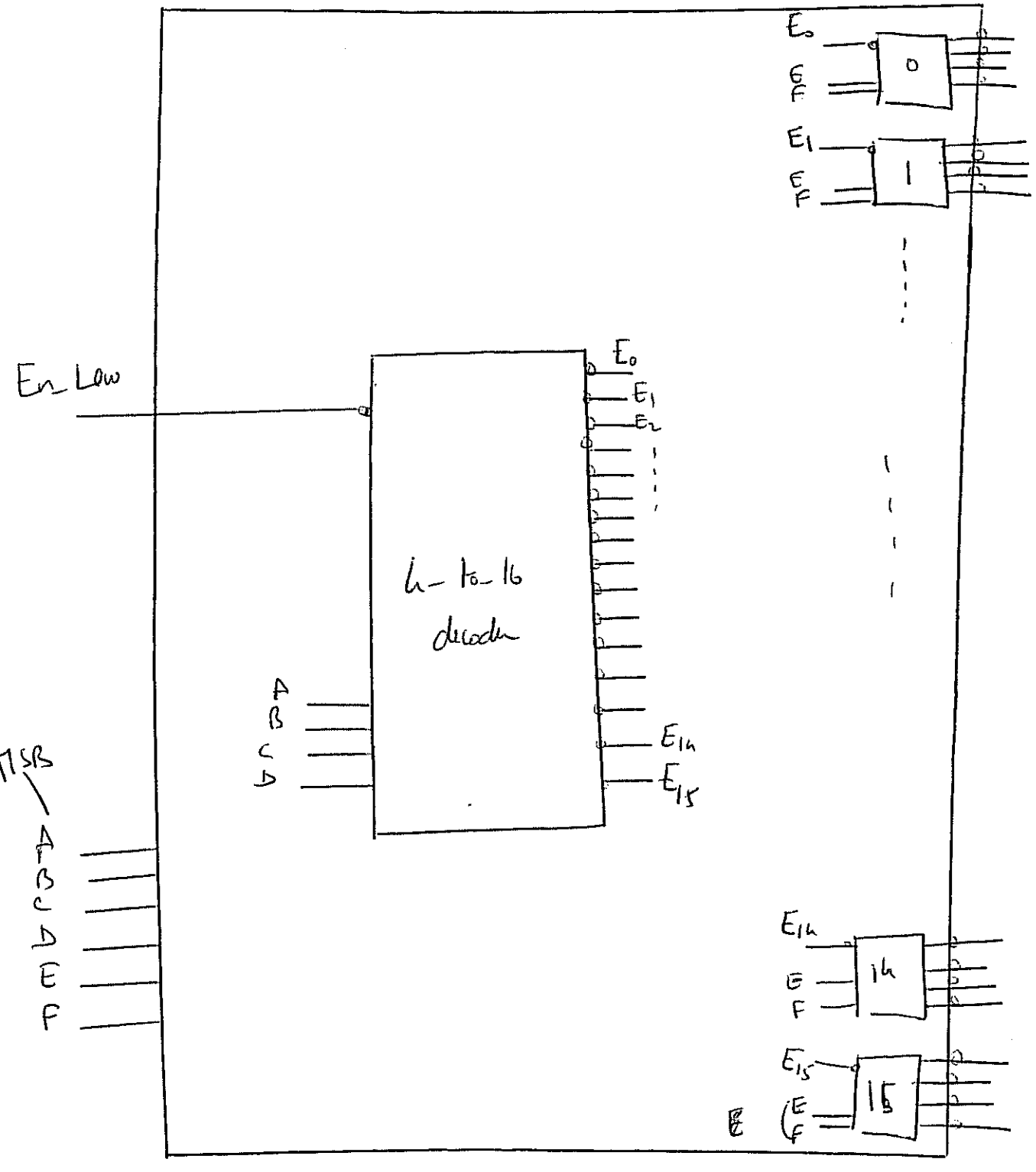
Assignment 5- Solution

Problem 1



Problem 2

```
library ieee
use ieee.std_logic_1164.all

entity decoder2to4 is
  port ( X: in std_logic_vector(1 downto 0);
         EN: in std_logic;
         Y: out std_logic_vector(0 to 3));
end decoder 2to4;

architecture behavioral of decoder 2to4 is
    signal Y_s : std_logic_vector(0 to 3);
begin
    Proces ( EN, X)
     begin
       Case X is
         when "00" => Y_s<="0111";
         when "01" => Y_s <="1011";
         when "10" => Y_s <="1101";
         when "11" => Y_s <="1110";
         when others => Y_s<="1111";

       end case

    if (EN='0')
      then Y<= Y_s;
    else Y <="1111";
    end if;
  end proces
```

(library ——

```
entity decoder_4to16 is
port ( X: in std_logic_vector(3 downto 0)
       EN: in std_logic;
       Y: out std_logic_vector(0 to 15));
end decoder 4 to 16;

architecture dataflow of decoder_4to16 is
    signal Y_s: std_logic_vector (0 to 16).
```

⋮

Check Code!

```
Library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY decoder2to4 IS
      Port ( X:  IN STD_LOGIC_VECTOR (1 DOWNTO 0) ;
             EN: IN STD_LOGIC;
           Y : OUT STD_LOGIC_VECTOR (0 TO 3)  ) ;
END decoder2to4 ;
ARCHITECTURE behavioral OF decoder2to4 IS
  SIGNAL Y_s : STD_LOGIC_VECTOR(0 TO 3) ;
BEGIN
      PROCESS( EN,X)
      BEGIN
           CASE  X IS
           WHEN "00"  =>  Y_s <=  "0111" ;
           WHEN "01"  =>  Y_s <=  "1011" ;
           WHEN "10"  =>  Y_s <=  "1101" ;
           WHEN "11"  =>  Y_s <=  "1110" ;
           WHEN OTHERS  =>  Y_s <=  "1111" ;
             END CASE ;
          IF ( EN) = '0'   THEN   Y <=(Y_s) ;
          ELSE   Y <= "1111" ;
          END IF ;
      END PROCESS;
END behavioral;
```

```
Library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Decoder4to16 is
  port (X: IN STD_LOGIC_VECTOR (3 DOWNTO 0);
        EN: IN STD_LOGIC;
        Y: OUT STD_LOGIC_VECTOR (0 to 15));
end Decoder4to16;

Architecture dataflow of Decoder4to16 is
  signal Y_s : STD_LOGIC_VECTOR(0 TO 15) ;
begin
     with X select Y_s <=
             "0111111111111111" when "0000" ,
             "1011111111111111" when "0001" ,
             "1101111111111111" when "0010" ,
             "1110111111111111" when "0011" ,
             "1111011111111111" when "0100" ,
             "1111101111111111" when "0101" ,
             "1111110111111111" when "0110" ,
             "1111111011111111" when "0111" ,
             "1111111101111111" when "1000" ,
             "1111111110111111" when "1001" ,
             "1111111111011111" when "1010" ,
             "1111111111101111" when "1011" ,
             "1111111111110111" when "1100" ,
             "1111111111111011" when "1101" ,
             "1111111111111101" when "1110" ,
             "1111111111111110" when "1111" ,
             "1111111111111111" when others;
            Y <= Y_s when (EN) = '1'   else
"1111111111111111";
end dataflow;
```

```
Library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Decoder6to64 is
  port (X: in STD_LOGIC_VECTOR (5 DOWNTO 0);
        EN: in STD_LOGIC;
        Y: out STD_LOGIC_VECTOR (0 TO 63));
end Decoder6to64;

architecture structural of Decoder6to64 is
  component Decoder2to4 port (X: IN STD_LOGIC_VECTOR (1 DOWNTO
0);
                              EN: IN STD_LOGIC;
                              Y: OUT STD_LOGIC_VECTOR (0 to
3));
  end component;
  component Decoder4to16 port(X: IN STD_LOGIC_VECTOR (3 DOWNTO
0);
                              EN: IN STD_LOGIC;
                              Y: OUT STD_LOGIC_VECTOR (0 to
15));
  end component;
  signal Y_internal: STD_LOGIC_VECTOR (0 to 15);
begin
  U0: Decoder4to16 port map (X(5 downto 2),EN,Y_internal);
  g2: for b in 0 to 15 generate
    U1: Decoder2to4 port map (X(1 downto 0), Y_internal(b), Y
(4*b to (4*b+3)));
  end generate;
end structural;
```

Problem 3

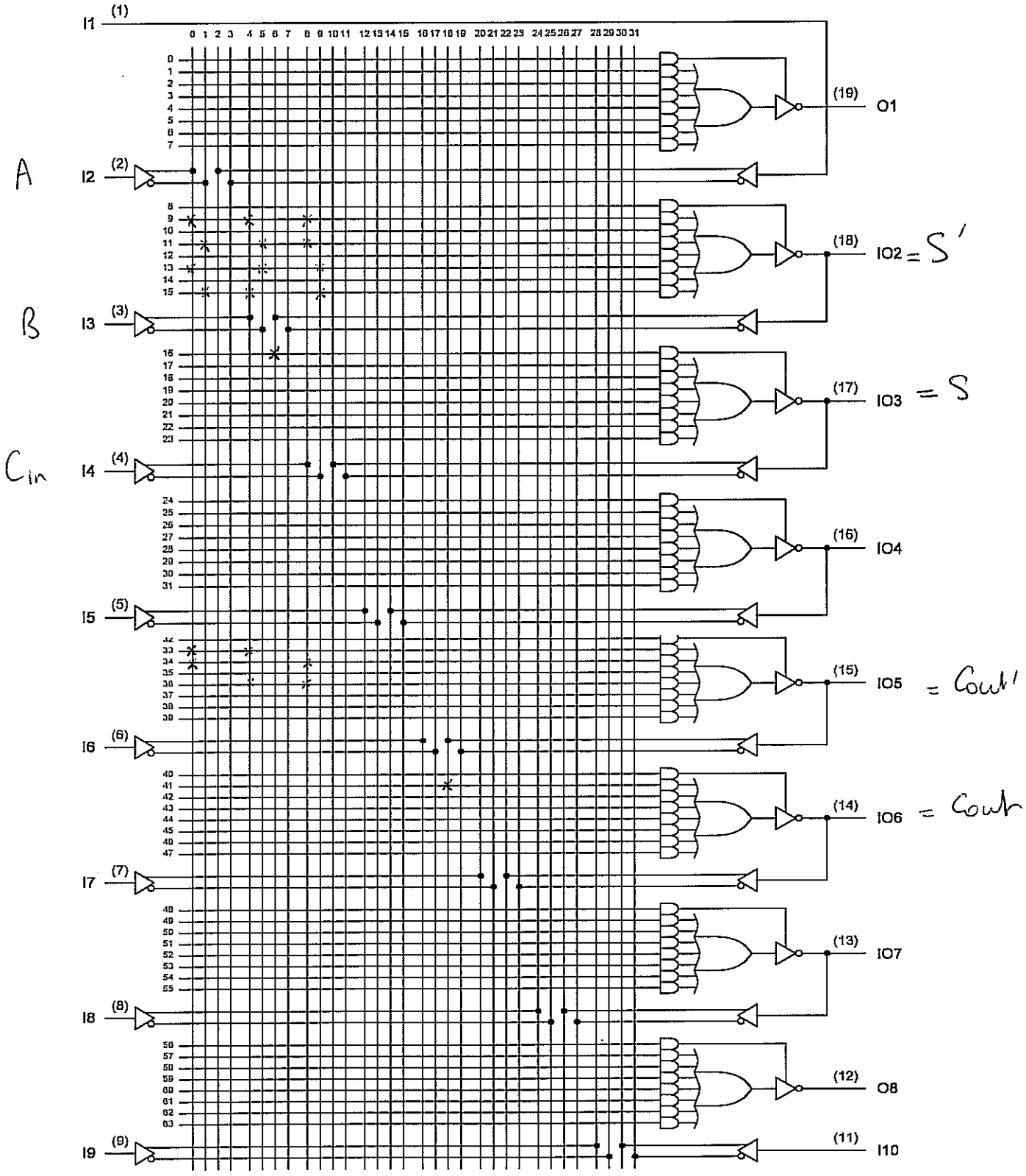
C_{in}	A	B	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S =$ ~~$A B C_{in} + A B C_{in}$~~

$A B C_{in} +$ ~~$A B$~~ $+$ ~~$A B$~~ $+ C_{in} A' B'$

$+ C_{in}' A B' + C_{in}' A' B$

$C_{out} = AB + A C_{in} + B C_{in}$


I1 (1)
A
I2 (2)
B
I3 (3)
Cin
I4 (4)
I5 (5)
I6 (6)
I7 (7)
I8 (8)
I9 (9)
(19) O1
(18) IO2 = S'
(17) IO3 = S
(16) IO4
(15) IO5 = Cout'
(14) IO6 = Cout
(13) IO7
(12) O8
(11) I10