## Problem 1: K-Map Minimization [6 points]

Minimize the following 5-variable Boolean function:

$$
\mathbf{F}=\Sigma_{\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D}, \mathbf{E}}(4,5,6,7,12,14,16,20,21,24,26,27,31)+\mathrm{d}(0,11,19,22,30)
$$



The minimum SOP of $\mathbf{F}$ is:

Problem 2: Design Using Multiplexers [6 points]
Design the function below using a 4-input multiplexer with control variables $\mathbf{A}$ and $\mathbf{B}$ and additional gates.

$$
\begin{aligned}
& \mathbf{F}=\mathbf{A}^{\prime} \mathbf{B}^{\prime} \mathbf{C}^{\prime} \mathbf{\mathbf { D } ^ { \prime }}+\mathbf{A}^{\prime} \mathbf{B}^{\prime} \mathbf{C}^{\prime} \mathbf{D}+\mathbf{A}^{\prime} \mathbf{B}^{\prime} \mathbf{C D}+\mathbf{A}^{\prime} \mathbf{B} \mathbf{C}^{\prime} \mathbf{D}+\mathbf{A}^{\prime} \mathbf{B} \mathbf{C D}^{\prime}+ \\
& \mathbf{A} \mathbf{B}^{\prime} \mathbf{C}^{\prime} \mathbf{D} \mathbf{D}^{\prime}+\mathbf{A} \mathbf{B}^{\prime} \mathbf{C}^{\prime} \mathbf{D}+\mathbf{A B} \mathbf{C}^{\prime} \mathbf{D}^{\prime}+\mathbf{A B} \mathbf{B} \mathbf{C}^{\prime} \mathbf{D}
\end{aligned}
$$

## Solution:

## Problem 3: PLA Design [6 points]

Draw the configuration of a 2 -input (A,B) PLA, with 2 outputs and 4 product terms. Show the connections needed in order to implement the functions:

$$
\begin{gathered}
\mathbf{F 1}=\mathbf{A} \text { XOR } \mathbf{B} \\
\mathbf{F 2}=\mathbf{A} \text { XNOR } \mathbf{B}
\end{gathered}
$$

## Solution:

## Problem 4: FSM Design [12 points]

Using a Moore machine with D flip-flops, design a sequence detector that would output a $\mathbf{Z}=1$ only after detecting the sequence $\mathbf{1 1 0 0}$ on its single input $\mathbf{X}$. Call the states $\mathbf{S 0}$, $\mathbf{S 1}$ etc. (Use don't cares for illegal states and use simplest state assignment.)
A. Draw the state diagram in the space below.
B. Fill as much as needed in the corresponding state and transition tables shown below.

|  | $\mathbf{X}$ |  |  |
| :---: | :---: | :---: | :---: |
| $\mathbf{S}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{Z}$ |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  | $S^{*}$ |  |  |


|  | $\mathbf{X}$ |  |  |
| :---: | :---: | :---: | :---: |
| Q1Q2Q3 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{Z}$ |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

C. The excitation equations are given by:



D1 = $\qquad$ $\mathrm{D} 2=$ $\qquad$ D3 = $\qquad$
$\qquad$
$\qquad$
$\qquad$

## Problem 5: FSM Design Using VHDL [12 points]

Write a VHDL code to implement the sequence detector of the previous question.
$\qquad$
$\qquad$
$\qquad$
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## Problem 6: Combinational Logic Design [12 points]

In this problem, you are asked to design a combinational logic system that converts a 4-bit "sign-andmagnitude" number ( $\mathbf{S M}_{\mathbf{2}} \mathbf{M}_{\mathbf{1}} \mathbf{M}_{\mathbf{0}}$ ) to a two's complement number ( $\mathbf{T}_{\mathbf{3}} \mathbf{T}_{\mathbf{2}} \mathbf{T}_{\mathbf{1}} \mathbf{T}_{\mathbf{0}}$ ).
a) First complete the following truth table.

|  | $\mathbf{S}_{\mathbf{M}}^{\mathbf{2}} \mathbf{\mathbf { M } _ { \mathbf { 1 } } \mathbf { M } _ { \mathbf { 0 } }}$ |  |  |  |  | $\mathbf{T}_{\mathbf{3}} \mathbf{T}_{\mathbf{2}} \mathbf{T}_{\mathbf{1}} \mathbf{T}_{\mathbf{0}}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| +0 | 0 | 0 | 0 | 0 |  |  |
| +1 | 0 | 0 | 0 | 1 |  |  |
| +2 | 0 | 0 | 1 | 0 |  |  |
| +3 | 0 | 0 | 1 | 1 |  |  |
| +4 | 0 | 1 | 0 | 0 |  |  |
| +5 | 0 | 1 | 0 | 1 |  |  |
| +6 | 0 | 1 | 1 | 0 |  |  |
| +7 | 0 | 1 | 1 | 1 |  |  |
| -0 | 1 | 0 | 0 | 0 |  |  |
| -1 | 1 | 0 | 0 | 1 |  |  |
| -2 | 1 | 0 | 1 | 0 |  |  |
| -3 | 1 | 0 | 1 | 1 |  |  |
| -4 | 1 | 1 | 0 | 0 |  |  |
| -5 | 1 | 1 | 0 | 1 |  |  |
| -6 | 1 | 1 | 1 | 0 |  |  |
| -7 | 1 | 1 | 1 | 1 |  |  |

b) Fill in each of the following four K-maps and minimize for sum of products implementation.

$\mathrm{T}_{1}$

$\mathrm{T}_{2}$

$\mathrm{T}_{0}$

| $\mathrm{T}_{3}=$ |
| :--- |
| $\mathrm{T}_{2}=$ |
| $\mathrm{T}_{1}=$ |
| $\mathrm{T}_{0}=$ |

## Problem 7: FSM Analysis [10 points]

A sequential circuit has three D flip-flops $A, B$, and $C$, and one input $X$. The circuit is described by the following input equations to the flip-flops. The variables $A, B$, and $C$, denote the current state variables ( $Q$-values) of the three flip-flops.

$$
\begin{aligned}
& D_{A}=\left(B C^{\prime}+B^{\prime} C\right) X+\left(B C+B^{\prime} C^{\prime}\right) X^{\prime} \\
& D_{B}=A \\
& D_{C}=B
\end{aligned}
$$

a) Derive the state transition table for the circuit.
b) Draw the corresponding state diagram.

## Problem 8: Arithmetic Unit [12 points]

In this problem, we'll design an $n$-bit ALU based on the following 1-bit full-adder block that takes as inputs $\mathbf{X}, \mathbf{Y}, \mathbf{C}_{\mathbf{i n}}$, and generates the sum $\mathbf{S}$ and carry out $\mathbf{C}_{\text {out }}$.

a) Write down Boolean equations for $\mathbf{S}$ and $\mathbf{C}_{\text {out }}$.

$$
\mathbf{S}=
$$

$\qquad$ $\mathrm{C}_{\text {out }}=$ $\qquad$
b) In this part, we want to use the adder to implement the following arithmetic operations specified by the control signals $\mathbf{M}_{2}, \mathbf{M}_{1}, \mathbf{M}_{\mathbf{0}}$. We add three logic blocks, $\mathbf{F}, \mathbf{G}, \mathbf{H}$, at the inputs of the adder to supply the appropriate arguments to perform the desired operation. Fill in the columns in the table below for values of $\mathbf{X}, \mathbf{Y}, \mathbf{C}_{\text {in }}$ required so that the adder generates the appropriate result. The first row has been completed for you. Hint: $\mathbf{- 1}$ in two's complement is represented as all ones.

| $\mathbf{M}_{\mathbf{2}}$ | $\mathbf{M}_{\mathbf{1}}$ | $\mathbf{M}_{\mathbf{0}}$ | Desired Operation $\mathbf{S}$ | $\mathbf{X}$ | $\mathbf{Y}$ | $\mathbf{C}_{\mathbf{i n}}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :---: |
| 0 | 0 | 0 | Add A and $\mathbf{B}$ | $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{0}$ |
| 0 | 1 | 0 | Add A' and B |  |  |  |
| 1 | 0 | 0 | Decrement A |  |  |  |
| 1 | 1 | 0 | One's complement of $\mathbf{A}$ |  |  |  |
| 0 | 0 | 1 | Subtract B from A |  |  |  |
| 0 | 1 | 1 | Subtract A from $\mathbf{B}$ |  |  |  |
| 1 | 0 | 1 | Increment $\mathbf{A}$ |  |  |  |
| 1 | 1 | 1 | Two's complement of $\mathbf{A}$ |  |  |  |


c) Using the results from the previous part, write down minimized Boolean equations for $\mathbf{X}, \mathbf{Y}$ and $\mathbf{C}_{\mathbf{i n}}$ in terms of $\mathbf{A}, \mathbf{B}, \mathbf{M}_{\mathbf{2}}, \mathbf{M}_{\mathbf{1}}, \mathbf{M}_{\mathbf{0}}$. Next, design the logic blocks $\mathbf{F}, \mathbf{G}, \mathbf{H}$.

Solution:

| Boolean equation for $\mathbf{X}$ |  |
| :---: | :---: |
|  |  |
|  |  |
|  |  |
| $X=\square$ |  |
|  |  |


| Boolean equation for $\mathbf{Y}$ |  |
| :---: | :---: |
|  |  |
|  |  |
|  |  |
|  |  |


| Boolean equation for $\mathbf{C}_{\text {in }}$ |  |
| :--- | :--- |
|  |  |
|  |  |
| $\mathbf{C}_{\mathbf{i n}}=\ldots$ |  |
|  |  |
|  |  |

## Problem 9: Arithmetic Unit [20 points]

The following questions are independent.
a) The following memories are specified by the number of words times the number of bits per word. How many address lines, input-output data lines are needed in each case, and how many bytes does each memory store: [4 points]

| Memory | Address lines | Input-Output lines | Number of bytes |
| :---: | :---: | :---: | :---: |
| $16 \mathrm{~K} \times 8$ |  |  |  |
| $256 \mathrm{~K} \times 16$ |  |  |  |
| $64 \mathrm{M} \times 32$ |  |  |  |
| $2 \mathrm{G} \times 8$ |  |  |  |

b) A $64 \mathrm{~K} \times 16$ RAM chip is designed in such a way that its cell array is square, i.e., it contains an equal number of bit-cells per row and column. A row decoder is used to select a row, and a column decoder is used to select the appropriate set of columns. Determine the following:
i. Number of bits in the cell array. [1 point]
ii. Size of the row decoder and the number of AND gates required to implement it. [3 points]
iii. Size of column decoder and the number of AND gates required to implement it. [3 points]
iv. If the input address $(076400)_{8}$ is applied to the chip, which row and column selection lines are enabled. Give your answers in decimal. [2 points]
c) A 256 Mb DRAM chip has a 4-bit data input bus and a 4-bit output data bus. Also, it has equal length row and column addresses. How many address pins does the DRAM have? [4 points]
d) How many 128 K x 16 DRAM chips are needed to provide memory capacity of 1 M bytes? How many address lines are required to access 1 M bytes? How many of these lines are connected to the address inputs of all chips? [3 points]

