American University of Beirut

Department of Electrical and Computer Engineering

EECE 311 – Electronic Circuits
Spring 2013
Final Exam – May 23, 2013
Open Book – 120 minutes

NAME:____________________________ **ID Number:** _______________________

- **Mark all your answers and ID number on the computer (Scantron) sheet.**
- **All problems are graded equally.**
- **There are 6 pages and 25 problems.**
- **Penalty is 5-to-1** (one to four wrong answers do not cancel a correct answer.)

PROBLEMS 1 – 6

Consider the logic gate circuit shown in Figure 1. Assume V_{DD} = 3.5 V. The MOSFET parameters are k_n' = 120 μA/V^2, k_p' = 60 μA/V^2, and $V_{tn} = -V_{tp}$ = 0.5 V. The NMOS transistor M_1 has $(W/L)_1$ = 6.8, while the PMOS transistor M_2 has $(W/L)_2$ = 3.4.
Note that when the PMOS M_2 is conducting, it is in the Saturation region.

The value of V_{OH} for this gate circuit is given by: $V_{OH} = V_{DD} - |V_{tp}|$.

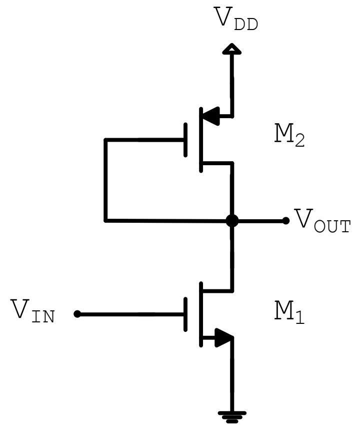

Figure 1

1. What is the logic function of this gate?
a) NAND b) NOT c) OR d) BUFFER e) NOR

2. Find the value of V_{OL} (in V)?
a) 0.424 b) 0.476 c) 0.273 d) 0.322 e) 0.373

3. Find the value of V_M (in V). At $V_{IN} = V_M$, $V_{OUT} = V_{IN} = V_M$.
a) 1.67 b) 1.0 c) 1.17 d) 1.33 e) 1.5

Assume in the following questions that $(W/L)_1$ is 19 and $(W/L)_2$ is unchanged at 3.4. This results in V_{OL} = 0.15 V.

4. Assuming that the input is low at V_{OL} 50% of the time, and high at V_{OH} 50% of the time, find the static power dissipation (in mW) of the circuit.
a) 0.436 b) 0.845 c) 1.45 d) 2.29 e) 3.40

5. The noise margin *NML* for this gate is $V_{DD}/4$. Find the value of V_{IL} (in V).
a) 1.275 b) 1.15 c) 0.90 d) 1.025 e) 0.775

A load capacitor of 0.2 pF is now connected from the output of the gate to ground.

6. How long (in nsec) does it take the output to rise from V_{OL} = 0.15 V to $V_{DD}/2$, when the input switches from V_{OH} to V_{OL} at t = 0. Use the average capacitor current method.
a) 1.08 b) 0.81 c) 0.65 d) 0.54 e) 0.46

PROBLEMS 7 – 11

The logic function $Y = \overline{A \bullet B \bullet (C + D) + E \bullet F}$ is to be implemented as a complex static CMOS gate, using a technology with V_{DD} = 2.0 V, k_n' = 250 μA/V^2, V_{tn} = 0.5 V, k_p' = 125 μA/V^2, and V_{tp} = –0.5 V.

7. Find the value of V_{OH} (in V) for this complex gate.
a) 1.4 b) 1.6 c) 1.8 d) 2.0 e) 1.2

8. How many transistors are needed to implement the complex gate?
a) 6 b) 9 c) 16 d) 15 e) 12

9. Find the (W/L) ratio of the MOSFET whose gate terminal is connected to input C in the PUN (pull-up network) if all transistors are sized properly, and given that the standard inverter has $n = (W/L)_N$ = 0.5 / 0.25 and $p = (W/L)_P$ = 1 / 0.25.
a) 3 / 0.25 b) 2 / 0.25 c) 0.5 / 0.25 d) 1.5 / 0.25 e) 1 / 0.25

10. Find the (W/L) ratio of the MOSFET whose gate terminal is connected to input A in the PUN (pull-up network) if all transistors are sized properly, and given that the standard inverter has $n = (W/L)_N$ = 0.5 / 0.25 and $p = (W/L)_P$ = 1 / 0.25.
a) 3 / 0.25 b) 2 / 0.25 c) 0.5 / 0.25 d) 1.5 / 0.25 e) 1 / 0.25

11. Find the dynamic power dissipation (in μW) of the CMOS gate when inputs A and C are low at 0 V (logic 0), inputs B, D, and E are high at V_{DD} (logic 1), and input F switches between 0 and V_{DD} (low and high) at a frequency of 1 MHz. A load capacitor of 0.5 pF is connected from the output of the gate to ground.

a) 2.0 b) 0.72 c) 0.98 d) 1.28 e) 1.62

PROBLEMS 12 – 13

An amplifier with three poles and no zeros has a low frequency open-loop voltage gain A_M = –1000 V/V. The first and dominant pole of this amplifier is ω_{p1}. The amplifier is used in a negative feedback configuration with a feedback factor β = 1.
Hint: Start by drawing the asymptotic Bode plot of the amplifier without feedback.

12. To stabilize the feedback amplifier, a **new** low-frequency pole is introduced at 5 Hz. Find the value of ω_{p1} (in krad/s).
a) 18.8 b) 25.1 c) 12.6 d) 6.28 e) 31.4

13. Assume ω_{p1} = 13000 rad/s. Instead of introducing a new low-frequency pole, the frequency of ω_{p1} may be shifted to a lower frequency. The pole at ω_{p1} is due to the input network, which is an RC circuit with a capacitance of 0.1 pF. The pole shifting is accomplished by introducing a new Miller capacitance between the input and the output of the amplifier. If the next pole frequency is 22 kHz, and assuming that all other poles/zeros are at much higher frequencies, what should be the Miller capacitance (in fF) needed to stabilize the feedback amplifier? (1 fF = 10^{-15} F).
a) 13.7 b) 9.3 c) 20.6 d) 17.1 e) 11.4

PROBLEMS 14 – 17

In the series-shunt feedback voltage amplifier shown in Figure 2, the current sources are ideal. Assume that MOSFET M_5 is biased such that it has g_{m5} = 0.5 mA/V and very large r_o. The other MOSFETs are biased such that the gain of the differential amplifier is v_{g5}/v_{sig} = 50 V/V, when the signal at the gate of transistor M_2 is zero.
The values of the resistors are: R_1 = 8 kΩ, and R_2 = 20 kΩ.
Use small-signal analysis with feedback techniques to analyze the circuit.

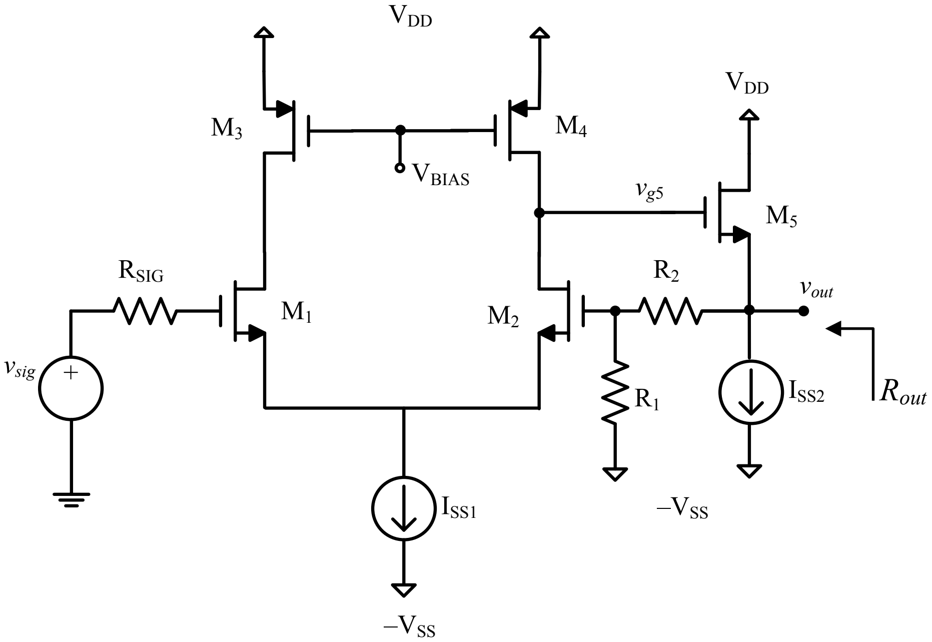

Figure 2

14. Find the value of the feedback factor β.
a) 0.200 b) 0.231 c) 0.259 d) 0.286 e) 0.310

15. Find the gain of the "modified A" circuit (in V/V), after breaking the feedback loop.
a) 46.5 b) 23.3 c) 84.9 d) 50.0 e) 34.2

16. Find the closed-loop gain of the feedback amplifier (in V/V).
a) 4.0 b) 3.6 c) 3.3 d) 3.0 e) 4.5

17. Find the output resistance of the feedback amplifier, R_{out} (in Ω).
a) 121 b) 130 c) 181 d) 159 e) 142

PROBLEMS 18 – 23

Figure 3 shows a CMOS op-amp circuit. All circuit elements are internal to the amplifier. Assume that $V_{DD} = 3$ V, $k'_n = 240$ μA/V^2, $k'_p = 110$ μA/V^2, $V_{tn} = 0.55$ V, $V_{tp} = -0.6$ V, and $I_{REF} = 65$ μA.

In *signal* analysis only, assume $V_{AN} = 16$ V, and $|V_{AP}| = 13$ V. **In *DC analysis*, neglect channel-length modulation.**

The sizes of the MOSFETs are as follows:

$(W/L)_1 = (W/L)_3 = (W/L)_6 = (W/L)_7 = (W/L)_8 = 12$
$(W/L)_2 = (W/L)_4 = (W/L)_5 = 24$
$(W/L)_9 = 5$

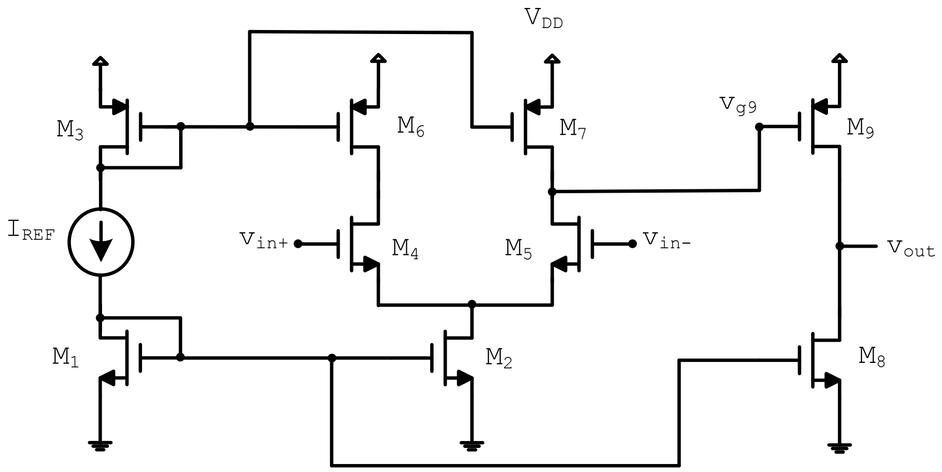

Figure 3

18. Find the differential input resistance (in kΩ) of the op-amp.
a) ∞ b) 0 c) 330 d) 1 e) 10^6

19. Find V_{OV} (absolute value, in V) of transistor M_9.
a) 0.504 b) 0.522 c) 0.447 d) 0.467 e) 0.486

20. Find the total power dissipation (in mW) in the circuit.
a) 0.66 b) 0.72 c) 0.78 d) 0.84 e) 0.90

21. Find the differential gain $v_{g9}/(v_{in+} - v_{in-})$ of the first stage in (V/V).
a) 44.4 b) 46.0 c) 49.7 d) 47.7 e) 51.9

22. Find the gain v_{out}/v_{g9} of the second stage (in V/V).
a) –30.7 b) –32.1 c) –29.5 d) –27.5 e) –28.4

23. The reference current source is implemented as a simple resistor (R_{REF}, replacing I_{REF}). What should be the value of R_{REF} (in kΩ) to obtain a reference current equal to I_{REF} flowing in the resistor?
a) 18.6 b) 20.4 c) 17.1 d) 24.8 e) 22.4

PROBLEMS 24 – 25

The op-amp used in Figure 4 is ideal, except for its open-loop gain, which is given by $A(s) = 10^8/(s + 100)$ V/V. Assume $R_1 = 1$ kΩ and $R_2 = 10$ kΩ.

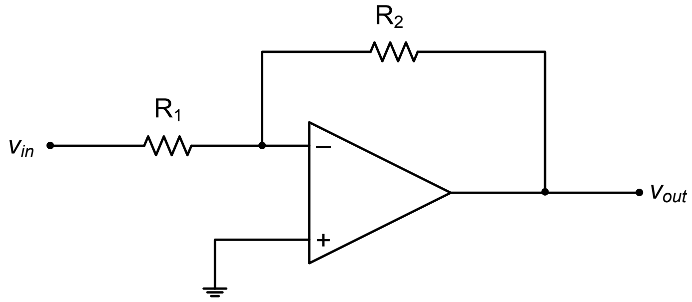

Figure 4

24. Find the low-frequency gain v_{out}/v_{in} (in V/V).

a) –10 b) –12 c) –15 d) –18 e) –22

25. Find the phase angle (in degrees) of $V_{out}(j\omega)/V_{in}(j\omega)$ at a frequency of 1 MHz.

a) 95 b) 108 c) 145 d) 121 e) 102