American University of Beirut
Department of Electrical and Computer Engineering
EECE 311 – Electronic Circuits
Spring 2010
Final Exam – June 5, 2010
Open Book – 180 minutes

NAME:_____ ID Number: _____

- **Mark all your answers and ID number on the computer (Scantron) sheet.**
- **All problems are graded equally.**
- **Penalty is 5-to-1** (one to four wrong answers do not cancel a correct answer.)

Consider the circuit shown in Figure 1. Assume V_{DD} = 2.5 V and R = 4 KΩ. The MOSFET parameters are k' = 200 μA/V^2, V_t = 0.5 V, and (W/L) = 5 μm / 0.25μm.

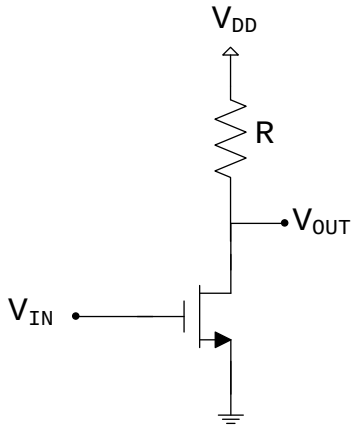


Figure 1

1. What is the logic function of this gate?
a) NOT b) BUFFER c) NOR d) NAND e) OR

2. When the input is low (below the threshold voltage of the MOSFET), what is the output high voltage, V_{OH} (in V)?
a) 1 b) 1.5 c) 2 d) 2.5 e) 0.5

3. What is the output low voltage, V_{OL} (in V), when the input voltage is at V_{OH}?
a) 0.15 b) 0.1 c) 0.08 d) 0.06 e) 0.3

4. Find the value of V_M (in V), at which $V_{IN} = V_{OUT}$.
a) 1.3 b) 1.1 c) 1.0 d) 0.94 e) 0.90

5. Find the value of V_{IL} (in V) for this gate.
a) 0.550 b) 0.750 c) 0.625 d) 0.583 e) 0.563

Assume in the following three problems that the resistor value in the circuit is changed to (991 Ω), such that the value of V_{OL} becomes equal to 0.3 V.

6. What is the average power dissipation of the gate (in mW)? Assume that the input voltage is high 50% of the time, and low 50% of the time.
a) 0.975 b) 1.44 c) 1.90 d) 2.34 e) 2.77

A load capacitor of 50 fF is now connected at the output of the gate.

7. At what time (in psec) does the output voltage reach 1.5 V, if the input switches from V_{OH} to V_{OL} at $t = 0$. *Hint*: Determine the region of operation of the MOSFET for $t > 0$.
a) 39.1 b) 63.0 c) 48.7 d) 134.7 e) 86.9

8. If the load capacitance increases from 50 fF to 100 fF, how would t_{PHL} change?
t_{PHL} increases by a factor of:

a) 100 b) 50 c) 2 d) 20 e) 5

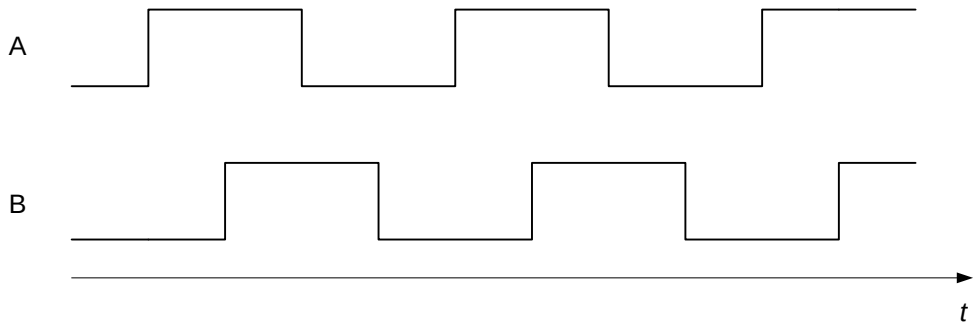
The logic function $Y = \overline{(A+B)\cdot(C+D)}$ is to be implemented as a complex static CMOS gate, using a technology with V_{DD} = 3 V, k_n' = 200 μA/V^2, V_{tn} = 0.5 V, k_p' = 100 μA/V^2, and V_{tp} = –0.4 V.

9. What is the total number of transistors needed?
a) 12 b) 10 c) 6 d) 4 e) 8

10. What is the size (width in μm) of the NMOS transistor whose gate terminal is connected to input *A*, if the standard inverter has $(W/L)_N$ = 0.3 μm / 0.2 μm.
a) 0.9 b) 0.3 c) 0.2 d) 1.2 e) 0.6

11. What is the static power dissipation (in μW) of the resulting complex gate, given the sizes of transistors as determined in Problem 10.
a) 0 b) 66.9 c) 45.6 d) 83.4 e) 12.7

12. Inputs *A* and *B* to the gate are square waves and switch at a frequency of 500 MHz as shown below (the waveforms are shifted with respect to one another by quarter of a period). If $C = \overline{A}$ and $D = \overline{B}$, find the dynamic power dissipation of the gate (in μW), if the gate is loaded by a 4 fF capacitor. *Hint*: First find the output waveform.



a) 90 b) 18 c) 36 d) 54 e) 72

The circuit shown in Figure 2 oscillates at a frequency of 19 KHz. The amplifier gain is $-K$ where K is a positive real number. The phase shifter block Φ introduces a phase shift but does not affect the magnitude of the signal passing through it.

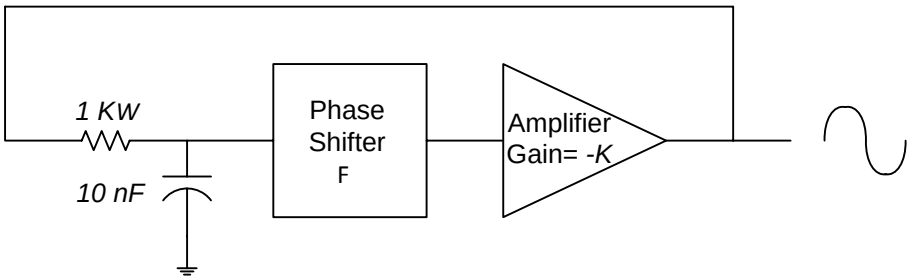


Figure 2

13. What is the phase shift (in degrees) introduced by the *RC* section, at the oscillation frequency? Neglect loading effects.
a) –54.1 b) –50.0 c) –32.1 d) –39.2 e) –45.2

14. What must be the phase shift (in degrees) introduced by the Φ block at the frequency of oscillation in the previous problem? Neglect loading effects.
a) –147.9 b) –140.8 c) –134.8 d) –129.9 e) –125.9

15. Find the minimum amplifier gain K needed to start oscillations.
a) 1.42 b) 1.56 c) 1.71 d) 1.18 e) 1.29

For the series-shunt feedback amplifier shown in Figure 3, assume that the MOSFET is biased such that g_m is 5 mA/V , and that channel-length modulation is negligible. Also assume that: R_D = 10 KΩ, R_1 = 100 KΩ, R_2 = 10 KΩ. Use feedback techniques to analyze the circuit.

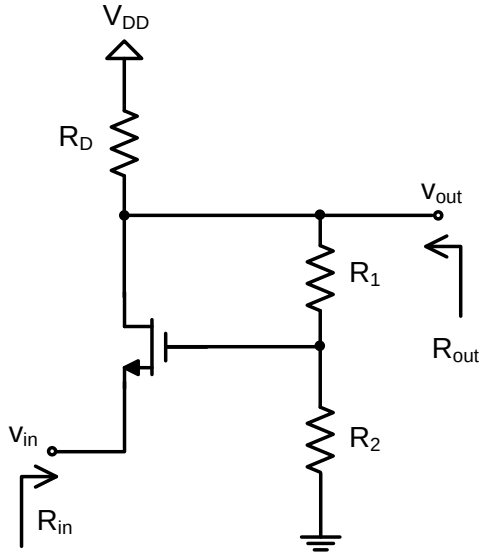


Figure 3

16. Find the gain of the "modified A" circuit, after breaking the feedback loop.
a) –24.2 b) –50 c) 24.2 d) 45.8 e) –45.8

17. Find the value of the feedback factor β.
a) 0.107 b) 0.083 c) 0.099 d) 0.091 e) 0.074

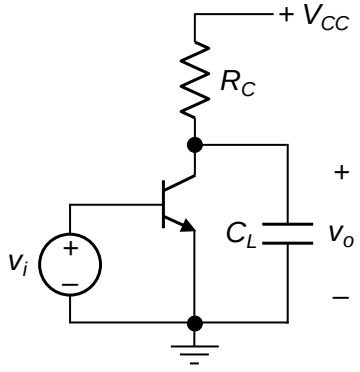
18. Find the closed-loop gain.
a) 9.58 b) 8.87 c) 8.27 d) 7.76 e) 10.4

19. Find the input resistance (in Ω) with feedback.
a) 878 b) 956 c) 1033 d) 1109 e) 1184

20. Find the output resistance (in Ω) with feedback.
a) 1551 b) 1774 c) 1654 d) 2085 e) 1916

---

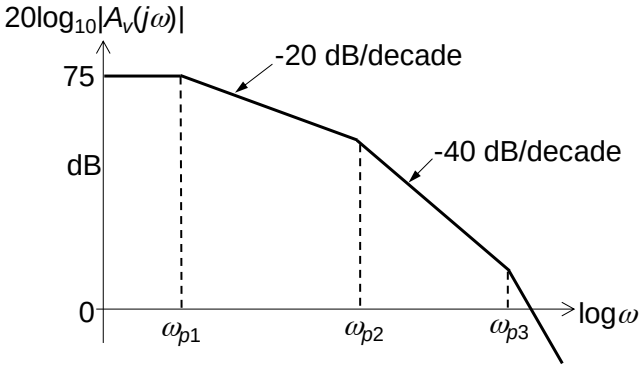
21. The transistor shown has g_m = 1.2 mA/V, r_π = 3 kΩ, r_o = 40 kΩ, C_μ = 2 pF, and C_π = 5 pF, with R_C = 10 kΩ and C_L = 8 pF.
The 3-dB cutoff frequency of the small-signal response v_o/v_i (in Mrad/s) is:



a) 10.4
b) 6.94
c) 12.5
d) 7.81
e) 5.68

---

22. The asymptotic magnitude Bode plot of the open-loop gain A_V of an amplifier is shown, where ω_{p1} = 300 krad/s, ω_{p2} = 6 Mrad/s, and ω_{p3} = 40 Mrad/s. The amplifier is to be used in a feedback configuration to provide a low frequency gain of nominally 10 (i.e. the feedback factor is β = 1/10 = 0.1). If the amplifier is stabilized using shifted pole compensation, the lowest pole frequency (in krad/s) becomes:

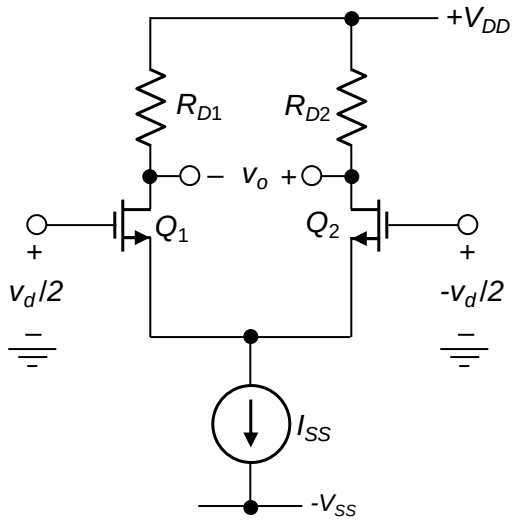


a) 3.56 b) 5.33 c) 7.11 d) 8.89 e) 10.67

---

23. It is given that g_{m1} = 1.2 mA/V, R_{D1} = 10 kΩ, g_{m2} = 1 mA/V, and R_{D2} = 19 kΩ, with r_{o1} and r_{o2} very large. The body effect can be neglected. The current source is ideal. The small-signal differential voltage gain v_o/v_d is: (*Hint*: use small-signal analysis.)

a) 12.5
b) 13.6
c) 14.7
d) 15.8
e) 16.9



24. In the circuit of the previous problem, the two MOSFET gates are now connected to a common input voltage v_{icm}. Find the common-mode gain, v_o/v_{icm}.
a) 0 b) –1 c) –1.2 d) –0.8 e) 0.8

25. The differential output resistance, across the v_O output, in the circuit of Problem 23 is (in kΩ):
a) 31 b) 29 c) 23 d) 27 e) 25
