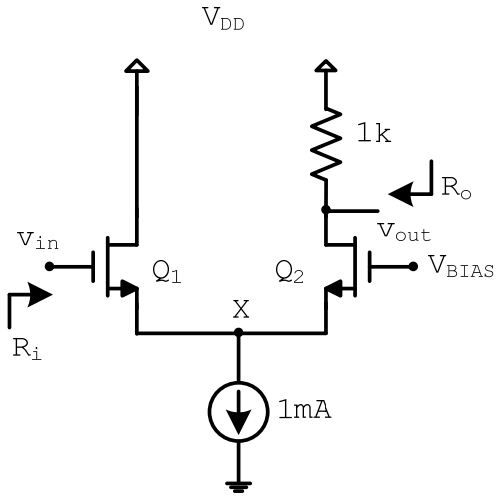
American University of Beirut
Department of Electrical and Computer Engineering
EECE 311 – Electronic Circuits
Summer 2009
Midterm – July 20, 2009
Open Book – 75 minutes

GRADE: / 40

NAME:_____ ID Number: _____

All questions are 2 points each.

In the circuit shown below, V_{DD} = 3 V and the two MOSFETs are identical and matched with W = 10 μm, L = 0.2 μm, V_t = 0.5 V, and k'_n = 200 μA/V^2. Neglect body effect and assume λ = 0.



The input v_{IN} is a small sinusoidal signal superimposed on a DC level equal to V_{BIAS} = 1.5 V. The same DC V_{BIAS} (without any signal) is also applied at the gate of MOSFET Q_2.

1) Find the DC drain currents in Q_1 and Q_2.

2) Find the values of V_{OV} and g_m for Q_1 and Q_2.

3) Find the DC voltage at node X, V_X.

4) If the signal at node X is considered the output of the Q_1 amplifier stage, determine the type of this amplifier (the first stage).

5) If the signal at node X is considered the input of the Q_2 amplifier stage, determine the type of this amplifier (the second stage).

6) Find the input resistance of the amplifier R_i.

7) Find the output resistance of the amplifier, R_o.

8) Find the small-signal voltage gain of the first stage, v_x/v_{in}. Hint: Use the T model.

9) Find the small-signal voltage gain of the second stage v_{out}/v_x.

10) What is the total amplifier voltage gain v_{out}/v_{in}, *in dB*?

The capacitances in the circuit are modeled as a load capacitor C_L = 25 fF that appears between the output of the amplifier and ground, and another capacitor C_X = 20 fF that appears between node X and ground.

Using the OCTC method:

11) Find the open-circuit resistance seen by C_L.

12) Find the open-circuit resistance seen by C_X.

13) Find the 3-dB frequency for the amplifier.

14) Show *and label* the magnitude Bode plot for the amplifier assuming a single pole at the frequency calculated in part (13).

Assume in the following that the 1 mA current source is implemented as a simple MOSFET current mirror.

15) Show the circuit implementation for such a current mirror. Name the mirror transistor Q_3, and assume that it is *identical* to Q_1 and Q_2.

16) What is the lowest possible voltage at node X to keep Q_3 saturated?

17) What is the output resistance of the current source if, for Q_3, $\lambda = 0.1\ V^{-1}$?

18) If the voltage at node X changes by +0.1 V, find the change in current for the current source.

19) The 1 kΩ resistor between the drain of Q_2 and the DC supply voltage is implemented as a MOSFET with gate connected to drain. Show how this MOSFET is connected.

20) Find the (W/L) ratio of the MOSFET in part (19) to get an equivalent small-signal resistance of 1 kΩ at a current level of 0.5 mA.