American University of Beirut

Department of Electrical and Computer Engineering

EECE 311 – Electronics II
Instructor: Ayman Kayssi
Final Exam
January 21, 2006

Open Book

Time: 180 minutes

Name:

ID Number:

Problem 1 [10 points]

a) Refer to the circuit shown in Figure 1. What should be the value of R in order to have class AB operation? Assume $|V_{BE(on)}| = 0.65$ V and neglect base current. Note that the bias circuit of Q_1 has negligible effect and is not shown.

b) The average DC current drawn from each of the two power supplies is 20 mA. What is the efficiency of the amplifier if the peak-to-peak output voltage is 10 V?

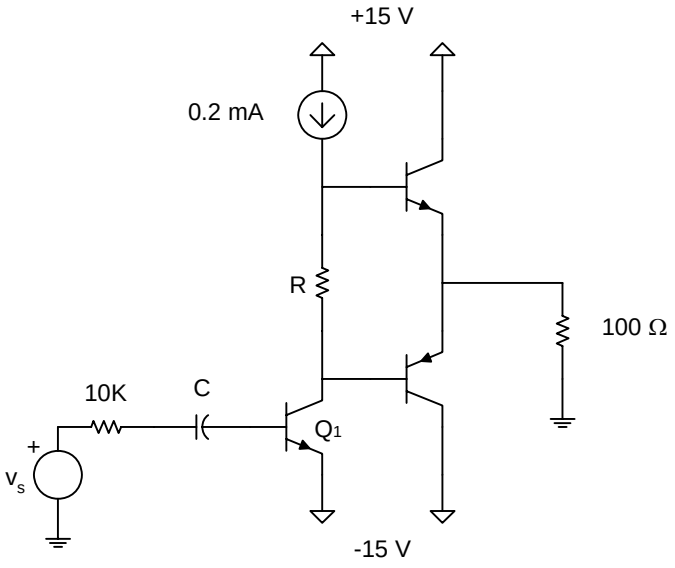

Figure 1

Problem 2 [20 points]

a) For the amplifier circuit shown in Figure 2, assume V_D = 0.7 V for a conducting diode, V_{BE} = 0.7 V, and $V_{CE(edge\ of\ sat)}$ = 0.3 V. The BJTs are identical and have negligible base current. The FETs are identical with $k'_n\,(W/L)$ = 2.5 mA/V^2 and V_t = 1 V. Find V_{OUT} when $V_1 = V_2 = 0$.

b) Find the total circuit power dissipation when $V_1 = V_2 = 0$.

c) Find the input common-mode range.

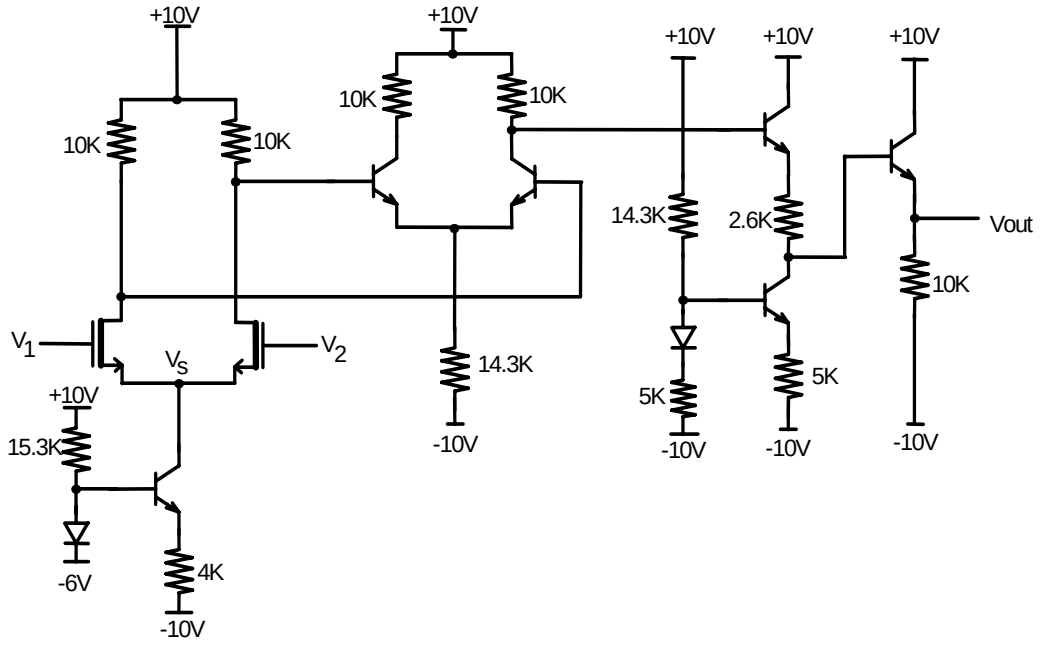

Figure 2

Problem 3 [20 points]

Consider the amplifier shown in Figure 3. For the MOSFET, g_m = 10 mA/V, and C_{gs} = C_{gd} = 0.1 pF. For the BJT, β = 100, g_m = 50 mA/V, C_π = 1 pF and C_μ = 0.5 pF.

a) Find the midband gain v_o/v_s.

b) Find the upper 3-dB frequency using Miller's theorem and the open circuit time constants method.

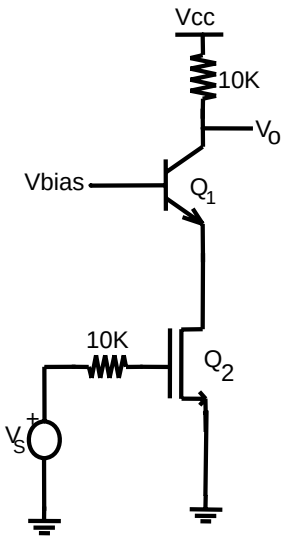

Figure 3

Problem 4 [20 points]

Design a low-pass Butterworth filter to meet the following specs:

A_{max} = 2.5 dB
A_{min} = 20 dB
f_P = 15 KHz
f_S = 25 KHz

Show the op-amp implementation of the filter. *Minimize* the number of op-amps in your implementation, and use 1 nF capacitors whenever possible.

Problem 5 [15 points]

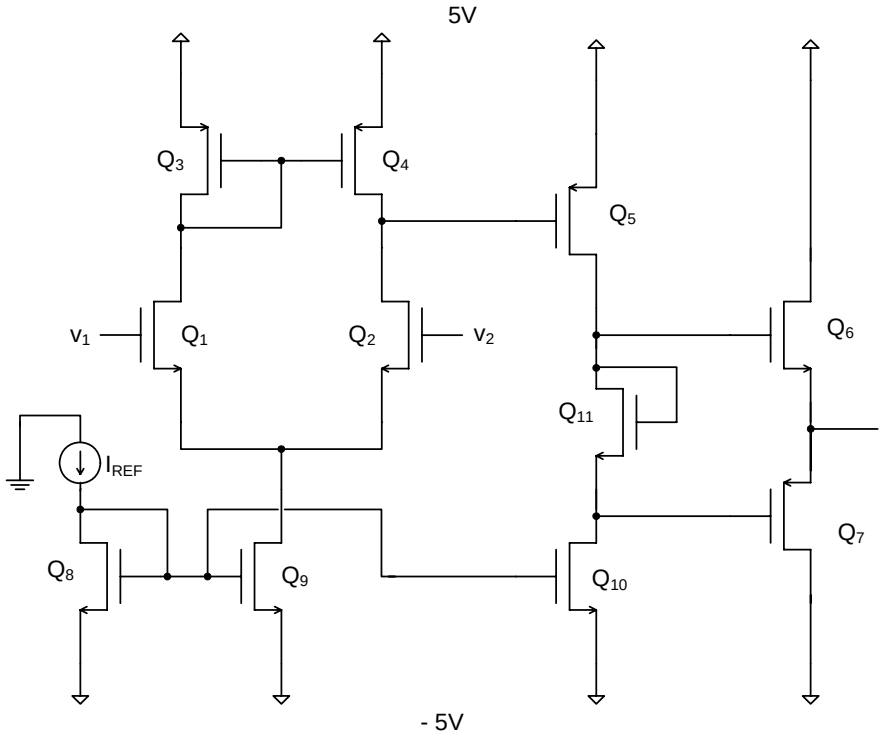

Figure 4

Consider the circuit shown in Figure 4.
a) What is the inverting input for this op-amp? Explain.

b) Find the output resistance of the op-amp. Assume that $k'_n = 25\ \mu A/V^2$, $k'_p = 10\ \mu A/V^2$, $V_{tn} = 0.75$ V, $V_{tp} = -0.75$ V, and $I_{REF} = 100\ \mu A$. The sizes of the MOSFETs are as follows: $(W/L)_1 = (W/L)_2 = (W/L)_9 = (W/L)_{10} = 20$
$(W/L)_3 = (W/L)_4 = 50$
$(W/L)_6 = (W/L)_8 = 10$
$(W/L)_5 = 100$
$(W/L)_7 = 25$
$(W/L)_{11} = 5$

Problem 6 [15 points]

The op-amp shown in Figure 5 is modeled by an infinite input resistance, an open-loop open-circuit differential voltage gain function of $\mathbf{10^7/(s+50)}$, and an output resistance of 500 Ω. What is the maximum load capacitance C_L that can be connected at the output of a voltage follower configuration (as shown in the figure), if the phase margin of the amplifier is 60 degrees?

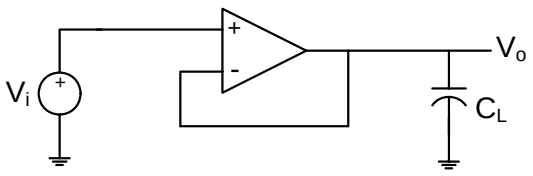

Figure 5