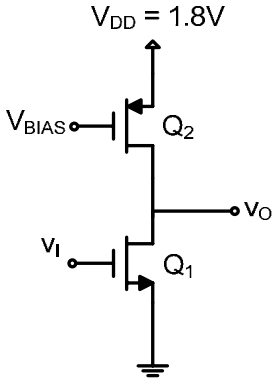
American University of Beirut
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
EECE 311 – Electronic Circuits (Sections 1 & 2)
Spring 2008

HOMEWORK 2
Due Wednesday March 12, 2008 at 1:00 PM

1. Common Source Amplifier

The common-source stage shown below must provide a voltage gain of 10 and has a power budget of 1 mW.



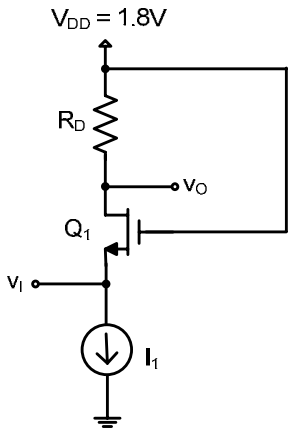
The technology parameters are: k'_n = 300 μA/V^2, V_{tn} = 0.45 V, V_{An} = 5 V, k'_p = 100 μA/V^2, V_{tp} = –0.5 V, and $|V_{Ap}|$ = 4 V.

Assume in the following that for the DC quantities: $I_D \simeq \frac{1}{2} k' \left(\frac{W}{L}\right) V_{OV}^2$.

a) Find the value of $(W/L)_1$
b) Find the required value of V_{BIAS} if $(W/L)_2$ is (20/0.18).

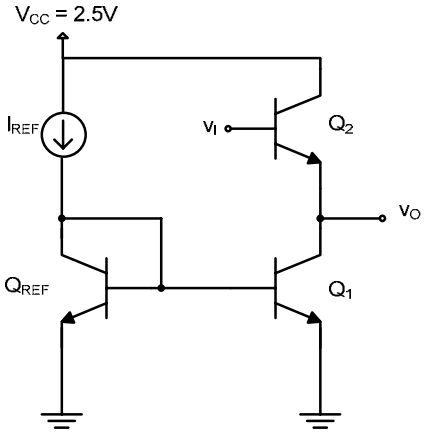
2. Common Gate Amplifier

Design the common-gate stage shown below for an input impedance of 50 Ω and voltage gain of 5. Assume a power budget of 2 mW. You should determine the aspect ratio (W/L) for the MOSFET, the value of R_D and the value of the current source I_1. The technology parameters are: k'_n = 300 μA/V^2 and V_{tn} = 0.45 V. *Neglect channel-length modulation*.



3. Emitter Follower

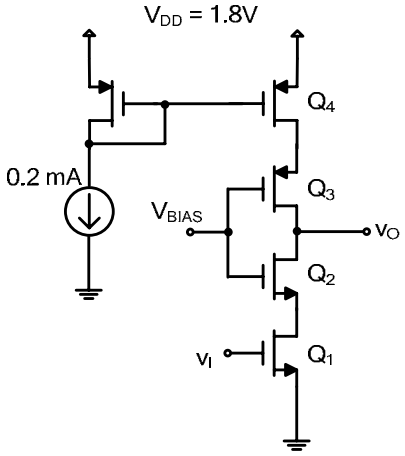
Design the emitter-follower circuit shown below for a power budget of 3 mW and an output impedance of 50 Ω. Neglect base width modulation, and assume that $\beta \to \infty$. Determine that value of I_{REF} and the value of the ratio $A_{E1}/A_{E\text{-}REF}$.



4. MOSFET Cascode

For the cascode circuit shown below, assume (W/L) = 10 μm/0.18 μm for all MOSFETs, and that V_{BIAS} = 0.9 V. Use PSpice to plot the input-output characteristics (v_o versus v_i). Note that the body terminals are connected to the supplies (ground for NMOS and V_{DD} for PMOS.) Determine from the plot the point at which the small-signal gain is maximum, in absolute value.

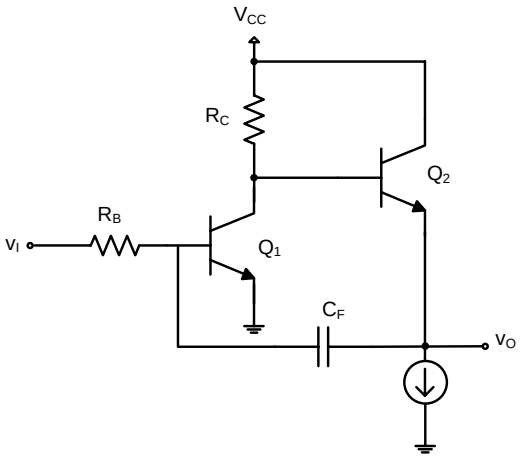
Now suppose the biasing circuitry that produces the above DC value of v_I incurs an error of +/– 20 mV. Explain what happens to the voltage gain.



Use the SPICE models posted on Moodle.

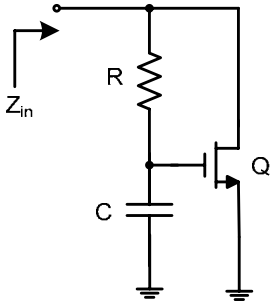
5. Miller's Theorem

Use Miller's theorem to estimate the input and output poles of the circuit shown below. Neglect base-width modulation and the internal BJT capacitors.



6. Active Inductor

The circuit shown below is called an active inductor. Neglecting all other capacitances, and channel-length modulation, compute the input impedance Z_{in}. Use Bode's rules to plot the magnitude of Z_{in} and explain how it exhibits inductive behavior.



7. Cascode Frequency Response

We wish to design the cascode circuit shown below for an input pole frequency of 5 GHz and an output pole frequency of 10 GHz. Assume Q_1 and Q_2 are identical, I_D = 0.5 mA, $C_{GS} = \frac{2}{3}W \times L \times C_{ox}$, C_{ox} = 12 fF/μm^2, $\mu_n C_{ox}$ = 100 μA/V^2, λ = 0, L = 0.18 μm, $C_{GD} = C_0 \times W$, where C_0 = 0.2 fF/μm. Determine the maximum allowable values of R_{sig} and R_D, and the voltage gain. Use Miller's approximation for C_{GD}. Assume an overdrive voltage of 200 mV for each MOSFET.