American University of Beirut

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING EECE 311 – Electronic Circuits (Sections 1 & 2) Spring 2008

HOMEWORK 4

Due Wednesday April 7, 2008 at 1:00 PM

Problem 1.

Calculate the differential voltage gain $v_{out}/(v_{in1}-v_{in2})$ in the circuit shown below. Assume perfect symmetry, but do *not* neglect channel length modulation. *Hint:* Use the half-circuit technique.



Problem 2.

The circuit shown below should provide a differential gain of 100 V/V at a power budget of 1 mW. Assume $V_{A,n} = 6$ V, $V_{CC} = 2.5$ V, and very large β .

- a) Find the bias current I_{EE} .
- b) Estimate $g_{\rm mN}$ and $r_{\rm oN}$.
- c) Calculate r_{oP} and estimate $V_{A,p}$.
- d) Estimate the input bias current if β_N is 200.
- e) Estimate the input offset current if β_N is matched to within +/-2%.



Problem 3.

Design the MOS differential amplifier shown in Figure 7.1 in the textbook for a differential voltage gain of 5 V/V and a power dissipation of 1 mW if the overdrive voltage must be at least 150 mV. Assume $k'_n = 100 \ \mu\text{A/V}^2$ and $V_{\text{DD}} = 1.8 \text{ V}$. Neglect channel length modulation. Find the values of *I*, *R*_D, and (*W/L*) for the MOSFETs.

Problem 4.

The differential amplifier shown below must provide a differential gain of 40 V/V. Assume that all transistors have the same overdrive voltage, and a circuit power budget of 2 mW. Also assume that $V_{res} = 10 \text{ V}$, $V_{res} = 5 \text{ W}$, $k'_{res} = 100 \text{ W} / V_{res}^2$, $k'_{res} = 50 \text{ W} / V_{res}^2$ and $V_{res} = 1.8 \text{ V}$.

- V_{A,n} = 10 V, V_{A,p} = 5 V, k'_n = 100 μA/V², k'_p = 50 μA/V², and V_{DD} = 1.8 V.
 a) Design the circuit by calculating the current I_{SS}, the overdrive voltage, and the (W/L) ratios of all MOSFETs.
 - b) Find the CMRR of the amplifier when the output is single-ended.



Problem 5.

Design the *telescopic* cascode amplifier shown below, for a differential voltage gain of 600 V/V with a power budget of 4 mW. Assume an overdrive voltage of 100 mV for the NMOS devices and 150 mV for the PMOS devices. Using $V_{A,n} = 10 \text{ V}$, $k'_n = 100 \text{ }\mu\text{A/V}^2$, $k'_n = 50 \text{ }\mu\text{A/V}^2$, and $V_{DD} = 1.8 \text{ V}$, determine the required value of $V_{A,p}$. Determine (*W/L*) for MOSFETs M₁ to M₈. Assume that M₁ – M₄ are identical, and so are M₅ – M₈.

