American University of Beirut
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
EECE 311 – Electronic Circuits (Sections 1 & 2)
Spring 2008

HOMEWORK 6
Due Wednesday May 28, 2008 at 1:00 PM

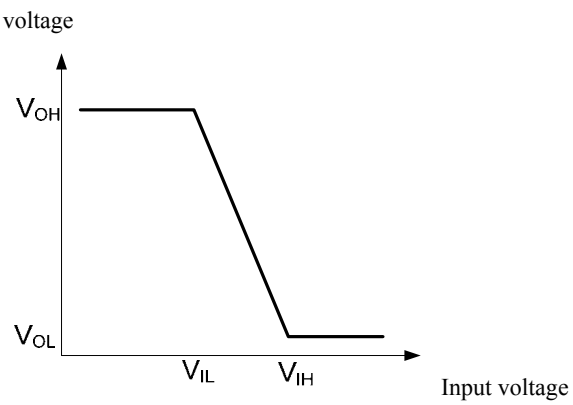
Problem 1.

For a certain logic-circuit family, the basic technology provides an inherent limit in the voltage gain of 40 V/V, maximum (in absolute value). If, with a 2 V supply, the values of V_{OL} and V_{OH} are ideal, but $V_M = 0.45V_{DD}$, what are the best possible values of V_{IL} and V_{IH}? What are the best possible noise margins? If the actual noise margins are 0.75 times these values, what V_{IL} and V_{IH} result? What is the large-signal voltage gain, defined as the absolute value of $(V_{OH} - V_{OL})/(V_{IH} - V_{IL})$?

Solution:

Ideal $V_{OH} = V_{DD} = 2$ V
Ideal $V_{OL} = 0$ V

VTC:



Slope in region between V_{IL} and $V_{IH} = -40$ V/V
Also: At $V_I = 0.45 \times V_{DD} = 0.9$ V, $V_O = 0.9$ V
Equation of straight line between V_{IL} and V_{IH}: $V_O = -40\ V_I + b$
$\Rightarrow b = 0.9 + 40(0.9) = 36.9$ V $\Rightarrow V_O = -40\ V_I + 36.9$ V
Intersection with $V_O = V_{OL} = 0$V level: $V_I = V_{IH} = 36.9/40 = 0.9225$ V
Intersection with $V_O = V_{OH} = 2$V level: $V_I = V_{IL} = (2-36.9)/(-40) = 0.8725$ V
Noise margins:
$NML = V_{IL} - V_{OL} = 0.8725$ V
$NMH = V_{OH} - V_{IH} = 2 - 0.9225 = 1.0775$ V

If the actual noise margins are 0.75 times these values:
$NML = V_{IL} - V_{OL} = V_{IL} = 0.75 \times 0.8725 = 0.654$ V
$NMH = V_{OH} - V_{IH} = 2 - V_{IH} = 0.75 \times 1.0775 = 0.808125$V $\Rightarrow V_{IH} = 1.192$ V
Large signal voltage gain = Slope = $(V_{OH} - V_{OL})/(V_{IH} - V_{IL}) = 2/(1.192-0.654) = 3.7$ V/V

Problem 2.

For a certain logic-circuit family, the standard inverter, when loaded by a similar circuit, has an average propagation delay of 30 ps.
a) If the current available to charge a load capacitance is half as large as that available to discharge the capacitance, what do you expect t_{PHL} and t_{PLH} to be?
b) When an external capacitive load of 25 fF is added at the inverter output, its propagation delay increases by 70% (i.e. by a factor of 1.7). What do you estimate the combined capacitance of inverter input and output to be?
c) If without the 25 fF load connected, and with the load inverter removed, the propagation delay is reduced by 40% (i.e. by a factor of 0.6), estimate the two components of capacitance found in (b).

Solution:

a) $t_P = 0.5\ (t_{PHL} + t_{PLH})$
If the current to charge the capacitor is half as large as the current to discharge it, this means that the time it takes to charge the capacitor is double the time it takes to discharge it. Therefore $t_{PLH} = 2\ t_{PHL}$.
30 ps = 0.5 (t_{PHL} + 2t_{PHL}) => t_{PHL} = 20 ps, and t_{PLH} = 40 ps.
b) t_P is proportional to C. Therefore $t_{P2} / t_{P1} = C_2 / C_1$ => 1.7 = (C_1+25 fF)/C_1 => C_1 = 25/0.7 = 35.7 fF = $C_{in} + C_{out}$. This is the combined capacitance of inverter input (load inverter) and output.

c) $t_{P3} / t_{P1} = 0.6 = (C_3 / C_1) = C_{out} /(C_{in} + C_{out}) = C_{out} / 35.7$ => C_{out} = 0.6×35.7 = 21.42 fF
=> C_{in} = 35.7 – 12.85 = 14.28 fF

Problem 3.

A CMOS microprocessor chip containing the equivalent of 10 million logic gates operates from a 1.8 V supply. The power dissipation is found to be 12 W when the chip is operating at 1.5 GHz, and 8 W when the chip is operating at 500 MHz.
a) What is the power lost in the chip by the some clock-independent mechanism, such as leakage and other static currents?
b) If 10% of the gates are assumed to be active at any time, what is the average gate load capacitance in such a design?

Solution:

a) $P_{dynamic}$ is proportional to the frequency f.
P_{static} is independent of f.
P_{total} is therefore given by $P_{total} = P_{dynamic} + P_{static} = a.f + P_{static}$
At 1500 MHz: $12 = a\times1500\times10^6 + P_{static}$
At 500 MHz: $8 = a\times500\times10^6 + P_{static}$
Therefore: $a = 4\times10^{-9}$ W/Hz, and $P_{static} = 8 – 4(0.5) = 6$ W.

b) $P_{dynamic}$ is assumed to be due to charging and discharging of load capacitances.
$P_{dynamic} = C_{switching}\ V_{DD}^2\ f$
$C_{switching}\ V_{DD}^2 = a = 4\times10^{-9}$
Therefore $C_{switching} = a / V_{DD}^2 = 4\times10^{-9}/1.8^2 = 1.23$ nF
This is the capacitance of 10% of the gates, that is 1 million gates.
Therefore, one gate capacitance is 1.23 nF / 1million = 1.23 fF.

Problem 4.

a) Use PSpice to simulate a CMOS inverter with $W_N = 0.24\mu m$, $L_N = 0.18\mu m$, $W_P = 1\mu m$, $L_P = 0.18\mu m$, in order to plot the voltage transfer curve (VTC), for $V_{DD} = 1.8$ V. Use the PSpice models posted on Moodle under Homework 2. Estimate using PSpice the noise margins and the value of V_M for this inverter.
b) Use PSpice to simulate the transient response of the CMOS inverter of part (a) when loaded by a 30 fF (0.03 pF) capacitance from output to ground. Use the following input waveform and transient analysis statements:

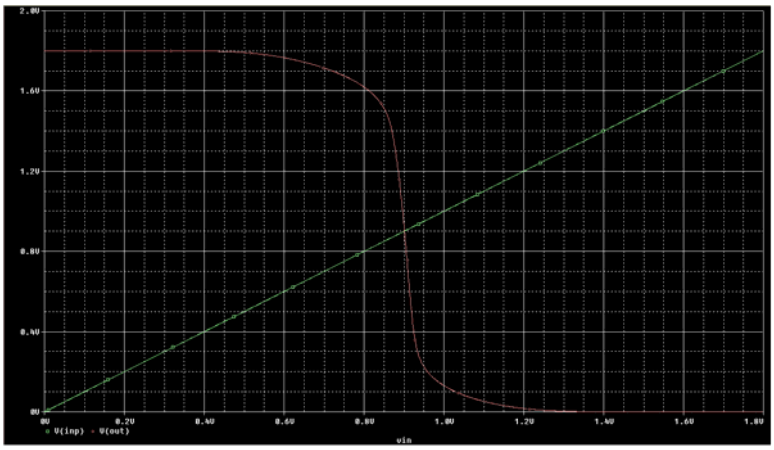
```
vin inp 0 pwl 0 0 0.1n 0 0.15n 1.8 1.2n 1.8 1.25n 0 2n 0
.tran 1p 2n
.options reltol=1e-7
```

Estimate the values of t_{PHL} and t_{PLH}. Also, estimate the energy gained/lost by the load capacitor during the low-to-high and high-to-low output transitions.

Solution

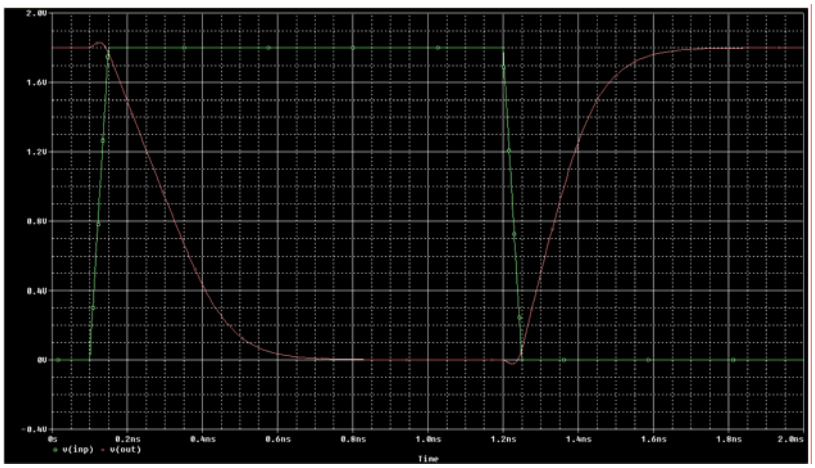
```
* cmos inverter
vdd pos 0 dc 1.8V
vin inp 0 0
* vin inp 0 pwl 0 0 0.1n 0 0.15n 1.8 1.2n 1.8 1.25n 0 2n 0
mn  out inp 0 0 cmosn l=0.18u w=0.24u
mp  out inp pos pos cmosp l=0.18u w=1u
.dc vin 0 1.8 1m
cload out 0 0.03p
* .tran 1p 2n
.options reltol=1e-7
.probe
* insert the TSMC mosfet models here
.end
```

The VTC is shown below.



V_M is very close to 0.9 V (0.901 V)
From the plot of D(V(out))
$V_{IL} = 0.763$ V => $NML = 0.763 - 0 = 0.763$ V
$V_{IH} = 1.0181$ V => $NMH = 1.8 - 1.0181 = 0.782$ V

From the transient response:



t_{PHL} = 182.2 ps
t_{PLH} = 124.1 ps

Energy in the capacitor can be calculated as follows: Plot `i(cload)*v(out)`, and then estimate the area under the curve, to find $\int Pdt$. Approximating the curve by a triangle, the area is around 5×10^{-14}Joules, which is close to the theoretical value of $\frac{1}{2} C V_{DD}^2$.

Problem 5.

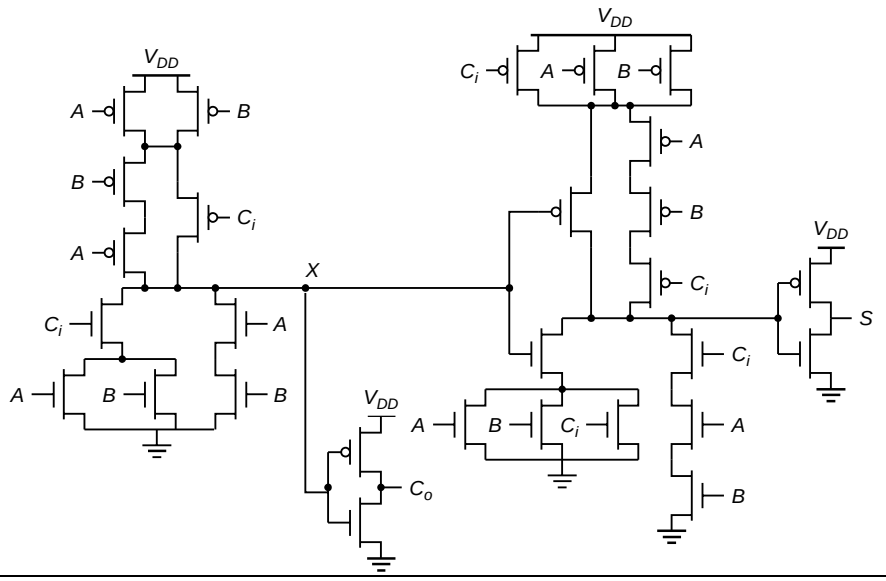
Design a CMOS full-adder circuit with inputs A, B, and C_{in}, and outputs S and C_{out}. The full adder output S is 1 if one or three inputs are 1, and C_{out} is 1 if two or more inputs are 1.

Solution:

$$S = A\cdot\overline{B}\cdot\overline{C_{in}} + \overline{A}\cdot B\cdot\overline{C_{in}} + \overline{A}\cdot\overline{B}\cdot C_{in} + A\cdot B\cdot C_{in}$$

$$C_{out} = A\cdot B + B\cdot C_{in} + A\cdot C_{in}$$

<u>*One*</u> possible static CMOS implementation that uses 28 transistors is shown below.



Problem 6.

Find appropriate sizes for the transistors used by the static CMOS XOR gate. Assume that the basic inverter has $(W/L)_N$ = 0.24μm/0.18μm and $(W/L)_P$ = 1μm/0.18μm. What is the total area, including the required inverters?

Solution:

The worst case in PUN and PDN are two MOSFETs in series. Therefore, all MOSFETs should be twice the size of the corresponding inverter MOSFET. The NMOS transistors should be 0.48μm/0.18μm and the PMOS transistors should be 2μm/0.18μm.

The total area is therefore:
4 NMOS transistors ×0.48μm×0.18μm +
4 PMOS transistors ×2μm×0.18μm +
area of two inverters (to invert the two inputs) =

4×0.48μm×0.18μm + 4×2μm×0.18μm + 2×(0.24μm×0.18μm +1μm×0.18μm) =
(4×0.48 + 4×2 + 2×0.24 + 2×1)×0.18 μm^2 =
2.232 μm^2

Problem 7.

Show pseudo-NMOS realization of the function $Y = \overline{A \cdot (B + C + D)}$.

Solution: