American University of Beirut
Faculty of Engineering and Architecture
Department of Electrical and Computer Engineering
EE 042 - Analog Electronics
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Quiz 1
Saturday November 23, 1996

Closed Book
Programmable Calculators Are Not Allowed.

Time: 1.5 hours

VERSION **A**

The figures for this quiz are missing

Name:_____ ID#:_____

- ❑ Provide your answer on the *computer card only*.
- ❑ Return the computer card attached to the question sheet.
- ❑ Use a pencil for marking your answers and ID number on the computer card.
- ❑ When using an eraser, make sure you erased well.
- ❑ On this sheet, write with a pen your name followed by your ID number.
- ❑ All questions are graded equally.

1. What is the version of your question sheet? (This question is not graded.)

   a) Version A
   b) Version B
   c) Version C
   d) Version D
   e) Version E

Unless otherwise specified, assume V_T = 25 mV, β is very large, and $|V_{BE}|$ = 0.7V

2. Determine R_C and R_E in the circuit of **Figure 8** to have V_O = 0V and V_{CE} = 3V. Assume β = 200 (do not neglect I_B).
   a) R_C = 0.82 kΩ, R_E = 1.65 kΩ
   b) R_C = 1.65 kΩ, R_E = 0.82 kΩ
   c) R_C = 1.82 kΩ, R_E = 0.65 kΩ
   d) R_C = 0.65 kΩ, R_E = 1.82 kΩ
   e) none of the above

3. Find the value of R required to satisfy the current relationships in the circuit of **Figure 7**.
   a) 100 kΩ
   b) 50 kΩ
   c) 200 kΩ
   d) 105 kΩ
   e) none of the above

4. For the circuit shown in **Figure 13**, find the voltage gain V_O/V_i. Assume β = 40, and r_π = 1 kΩ.
   a) -33.7
   b) -28.3
   c) -14.6
   d) -3.51
   e) none of the above

5. Find the current gain I_O/I_i directly, as defined in the circuit of **Figure 12**. The JFET parameters are I_{DSS} = 4mA and V_P= -2V and is biased at I_D = 1mA.
   a) -340
   b) -680
   c) -170
   d) -425
   e) none of the above

6. A MOSFET source follower is biased at I_D = 0.5mA. What is the value of V_{GS} if the small signal output resistance is 500Ω and V_t = 1V.
   a) 2.2 V
   b) 2 V
   c) 1.5 V
   d) 1.2 V
   e) none of the above

7. Find the differential gain $v_O/(v_1-v_2)$ in the circuit of **Figure 4**.
   a) -100
   b) -200
   c) 200
   d) 100
   e) none of the above

8. Find the common-mode rejection ratio (CMRR) for the circuit of **Figure 4**.
Assume $V_A = 100V$.

a) 73 dB
b) 82 dB
c) 66 dB
d) 78 dB
e) none of the above

9. Find the value of the emitter resistors, to be inserted between the emitters of Q_1 and Q_2 and node X in the circuit of **Figure 4**, to have a differential input resistance of 200KΩ. Assume $\beta = 99$.

a) 1.5 kΩ
b) 5 kΩ
c) 150 Ω
d) 35 Ω
e) none of the above

10. Find the value of R in the circuit of **Figure 3** in order to have $V_O = 2V$.

a) 7.17 kΩ
b) 9.5 kΩ
c) 14.3 kΩ
d) 19 kΩ
e) none of the above

11. All the BJTs in the circuit of **Figure 9** are biased at I_C=1mA and have $\beta = 100$. Find V_O/V_3 and V_3/V_2. (*Hint*: Include the loading effect of the last stage on the second stage).

a) $V_O/V_3 = -60$, $V_3/V_2 = 0.985$
b) $V_O/V_3 = -80$, $V_3/V_2 = 0.994$
c) $V_O/V_3 = -60$, $V_3/V_2 = 0.994$
d) $V_O/V_3 = -80$, $V_3/V_2 = 0.985$
e) none of the above

12. Find V_O/V_S in the circuit of **Figure 9**.

a) 540.5
b) 187.4
c) 932.6
d) 349.1
e) none of the above

13. Find the range of values of I_O in the circuit of **Figure 2**, when β varies between 75 and 175.

a) 0.918 to 0.925 mA
b) 0.459 to 0.462 mA
c) 0.468 to 0.471 mA
d) 0.926 to 0.931 mA
e) none of the above