American University of Beirut

Department of Electrical and Computer Engineering

EECE 311 – Electronic Circuits

Spring 2008

Midterm – April 11, 2008

Open Book – 90 minutes

NAME:_____________________________ **ID Number:** _______________________

Problem 1 [60 points]

Mark the answers for questions 1 to 15 below on the Scantron (computer) sheet.

Consider the circuit shown in Figure 1. Assume V_{DD} = 2.5 V. The MOSFET parameters are k' = 200 µA/V^2, V_t = 0.5 V, $(W/L)_1$ = 20µm / 0.25µm, and $(W/L)_2$ = 10µm / 0.25µm. Assume that the DC drain current of a MOSFET in SAT is given by $I_D \simeq \frac{1}{2}k'\left(\frac{W}{L}\right)V_{OV}^2$.

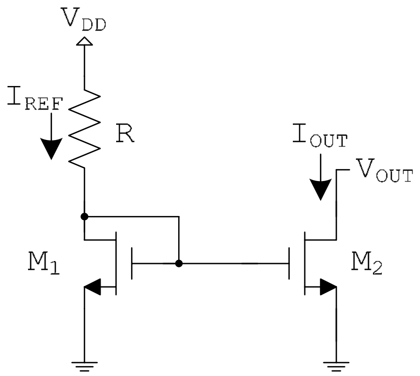


Figure 1

1. [4 points] Find the resistance R (in KΩ) in the circuit if the current I_{REF} is 100 µA.

a) 6.02 b) 18.88 c) 12.42 d) 9.21 e) 7.29

2. [4 points] Find the drain current of M_2, I_{OUT} (in µA).

a) 75 b) 100 c) 125 d) 150 e) 50

3. [4 points] Find the largest resistance (in KΩ) that can be connected between the drain of M_2 and V_{DD} to maintain saturation region operation for M_2.

a) 15.38 b) 23.42 c) 47.76 d) 31.51 e) 18.59

4. [4 points] Find the variation in I_{OUT} (in µA) when V_{OUT} increases from 1.5 to 2.5 V. At L = 0.25 µm, V_A is 10 V.

a) 5 b) 7.5 c) 10 d) 12.5 e) 15

5. [4 points] Repeat question 4, assuming that $(W/L)_2$ is changed from 10μm / 0.25μm to 40μm / 1μm.

a) 3.75 b) 1.25 c) 1.88 d) 2.50 e) 3.13

6. [4 points] A P-channel MOSFET M_3 with $k' = 100$ μA/V^2, and $V_t = -0.6$ V is connected with MOSFET M_1 of question 1, as shown in Figure 2. Find $(W/L)_3$ if the current I_{REF} is 200 μA and $R = 4.5$ KΩ.

a) 108.6 b) 34.2 c) 46.9 d) 68.4 e) 20.5

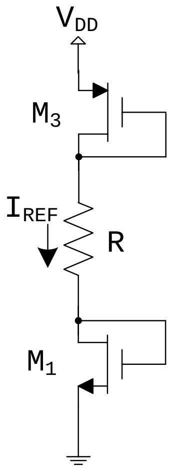


Figure 2

Consider the differential amplifier shown in Figure 3. The reference current is $I_{REF} = 240$ μA. Assume $V_{DD} = 2.5$ V. The MOSFET parameters are as follows.

For NMOS:
$k'_n = 200$ μA/V^2, $V_{tn} = 0.5$ V
$(W/L)_1$ = 20μm / 0.25μm
$(W/L)_2$ = 10μm / 0.25μm
$(W/L)_4$ = 10μm / 0.25μm
$(W/L)_5$ = 10μm / 0.25μm

For PMOS:
$k'_p = 100$ μA/V^2, $V_{tp} = -0.6$ V
$(W/L)_3$ = 40μm / 0.25μm
$(W/L)_6$ = 10μm / 0.25μm
$(W/L)_7$ = 10μm / 0.25μm

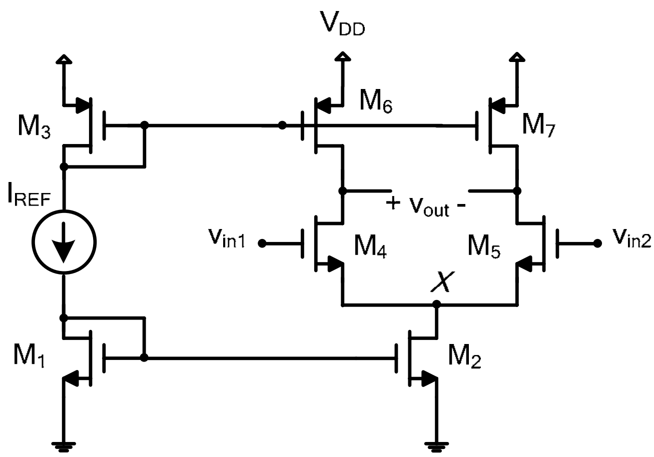


Figure 3

7. [4 points] Find the DC voltage (in mV) at node X when the two inputs are at 0.9 V.

a) 258.6 b) 250.0 c) 277.5 d) 267.7 e) 288.2

8. [4 points] Find the total power dissipation (in mW) in the circuit.

a) 0.90 b) 1.05 c) 1.20 d) 1.35 e) 0.75

Assume in the following that V_{AN} = 10 V, *and* $|V_{AP}|$ = 8 V.

9. [4 points] Find the small-signal differential gain $v_{out}/(v_{in1} - v_{in2})$.

a) –79.5 b) –72.6 c) –67.2 d) –62.9 e) –59.3

10. [4 points] Find the small-signal differential gain $v_{out}/(v_{in1} - v_{in2})$ when a 1000 KΩ resistor is connected across the v_{out} terminals.

a) –53.9 b) –56.6 c) –67.5 d) –63.2 e) –59.6

11. [4 points] Find the small-signal common-mode gain when the output is taken *single-endedly* (at the drain of M_4 or M_5). In this case, $v_1 = v_2 = v_{icm}$.

a) –2.8 b) –0.008 c) –0.08 d) –0.8 e) –1.8

12. [4 points] Find the small-signal common-mode gain when the output is taken differentially. In this case, $v_1 = v_2 = v_{icm}$.

a) 0 b) 0.08 c) –0.08 d) –0.008 e) 0.008

Assume in the following two questions that when the input is common-mode, the DC voltage at the drains of M_4 *and* M_5 *is* 1.5 V.

13. [4 points] Find the maximum common-mode input voltage (in V) that maintains saturation-region operation for all MOSFETs in the circuit.

a) 2.4 b) 2.0 c) 2.1 d) 2.2 e) 2.3

14. [4 points] Find the minimum common-mode input voltage (in V) that maintains saturation-region operation for all MOSFETs in the circuit.

a) 0.86 b) 0.80 c) 0.82 d) 0.84 e) 0.77

15. [4 points] The two inputs are $v_{in1}(t) = 4.5\sin(\omega t)$ mV and $v_{in2}(t) = 4.9\sin(\omega t)$ mV. If the differential gain is 62 dB, and the CMRR is 50 dB, find the amplitude of the output voltage (in V).

a) 0.52 b) 0.33 c) 0.37 d) 0.41 e) 0.47

Problem 2 [40 points]

Solve this problem on the answer booklet.

The common-emitter amplifier shown in Figure 4 is biased using I_{REF} = 140 μA, and has V_{An} = 10 V, $|V_{Ap}|$ = 5 V, and large β. Q_2 and Q_3 are matched. In DC analysis, assume that the collector current in ACTIVE is given by $I_C \simeq I_S e^{\frac{V_{BE}}{V_T}}$, where V_T = 25 mV.

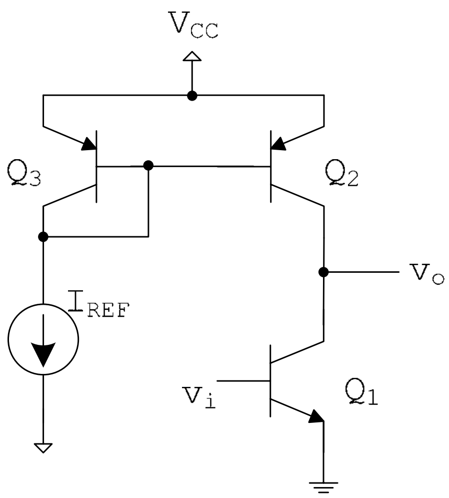


Figure 4

a) [5 points] Find the output resistance of the amplifier. Assume all transistors are an *internal part* of the amplifier.

The output resistance is $r_{o(Q1)}$ // $r_{o(Q2)}$
Since Q_2 and Q_3 are matched, and β is very large: $I_{C1} = I_{C2} = I_{REF}$ = 140 μA.
$r_{o(Q1)} = V_{AN} / I_{C1}$ = 10/0.14 = 71.43 KΩ
$r_{o(Q2)} = |V_{AP}| / I_{C1}$ = 5/0.14 = 35.71 KΩ
Rout = $r_{o(Q1)}$ // $r_{o(Q2)}$ = 71.43 // 35.71 = 23.81 KΩ

b) [5 points] Find the open-circuit voltage gain v_o/v_i.

The open circuit voltage gain v_o/v_i is $-g_{m1} R_{out}$
$g_{m1} = I_{C1}/V_T$ = 0.14/25 = 5.6 mA/V
$v_o/v_i = -g_{m1} R_{out}$ = –5.6 × 23.81 = –133.34 V/V

Assume in the following that a signal source is connected to the input of the amplifier. It is a voltage source v_{sig} with a source resistance R_{sig} = 25 KΩ. Assume also that a 10 KΩ load resistor is connected from the output to ground. The signal source and the load do not affect the DC bias.

c) [4 points] Find the input resistance v_i/i_i of the amplifier if β = 200.

The input resistance v_i/i_i is $r_\pi = V_T/I_B = \beta V_T/I_C$ = 200 × 25/0.14 = 35.71 KΩ

d) [4 points] Find the voltage gain v_o/v_{sig}.

The voltage gain is $-g_{m1} R'_L$ × (voltage divider ratio at input).

$R'_L = R_{out} // R_L$ = 23.81 // 10 = 7.04 KΩ
The voltage divider ratio at the input is $r_\pi / (r_\pi + R_{sig})$ = 35.71 / (35.71+25) = 0.5882

The voltage gain v_o/v_{sig} = –5.6 × 7.04 × 0.5882 = –23.19 V/V

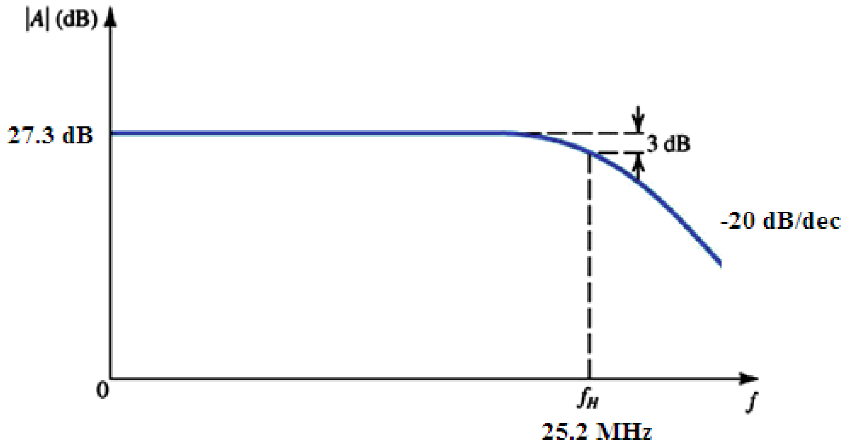
Assume now that for Q_1, C_π = 25 fF, C_μ = 10 fF, and that a load capacitance C_L = 40 fF is connected from the output to ground. Neglect all other capacitances.

e) [5 points] Using Miller's theorem, and assuming that the input circuit determines the upper 3-dB frequency f_H, find the value of f_H.

The Miller constant K is $v_c/v_b = -g_{m1} R'_L$ = –5.6 × 7.04 = –39.42
We apply Miller's theorem to obtain the input capacitance:
The input capacitance is $C_{in} = C_\pi + (1 - K)C_\mu$ = 25 + (1+39.42) ×10 = 429.2 fF
The resistance seen by this input capacitance is $r_\pi // R_{sig}$ = 35.71 // 25 = 14.71 KΩ
The 3-dB frequency due to the input circuit is
$f_H = 1/(2\pi\ C_{in}\ (r_\pi // R_{sig}))$ = 1/(2π × 429.2 f × 14.71 K) = 25.21 MHz

f) [5 points] Based on the results of (d) and (e), show and *label* the Bode plot for the magnitude of the voltage gain (v_o/v_{sig}).

The low-frequency gain is –23.19 V/V, which corresponds to 27.3 dB
The 3-dB frequency is 25.21 MHz



g) [12 points] Using the open-circuit time constants methods, find the resistance seen by each capacitor [3 points each], and estimate the value of f_H [3 points].

R(seen by C_π) $= r_\pi // R_{sig}$ = 14.71 KΩ
R(seen by C_L) $= R'_L$ = 7.04 KΩ
R(seen by C_μ) $= (r_\pi // R_{sig}) + R'_L + g_{m1} R'_L(r_\pi // R_{sig})$ frequently-used resistance calc.
= 14.71 + 7.04 + 5.6 × 14.71 × 7.04
= 601.7 KΩ

f_H = 1/(2π(25f×14.71K + 40f×7.04K + 10f×601.7K)) = 23.87 MHz