American University of Beirut
Department of Electrical and Computer Engineering
EECE 311 – Electronics II
Fall 2005 – 2006 (Section 2)
Quiz 2 – December 22, 2005
Closed Book – 90 minutes

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I have neither given nor received aid on this exam
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Problem 1 [40 points]

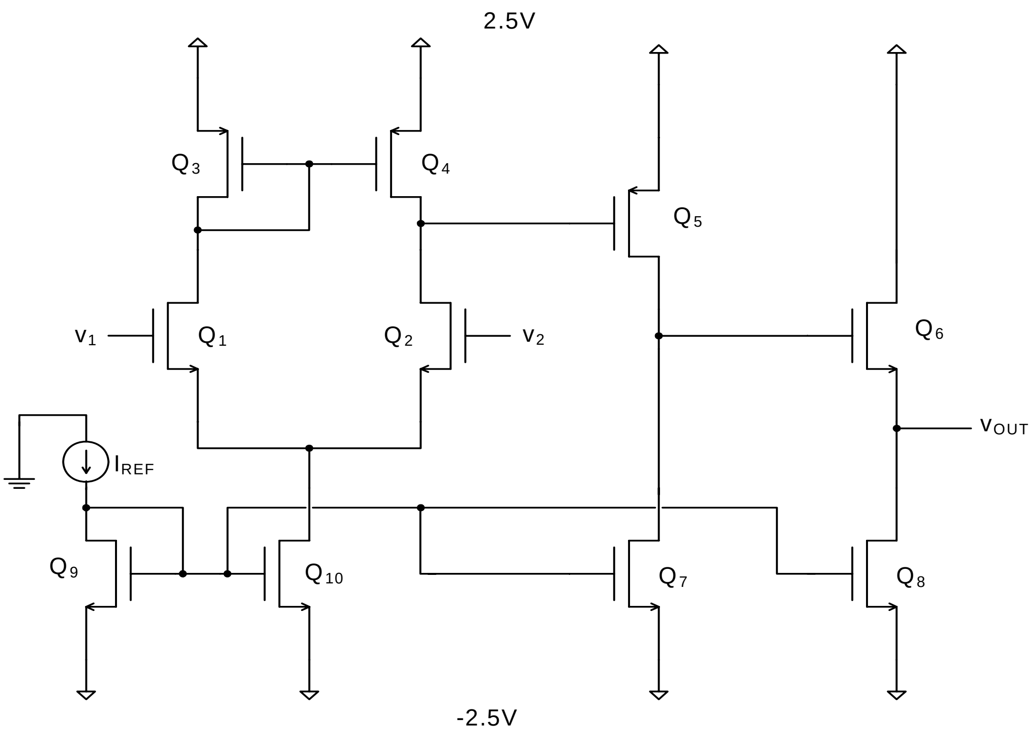


Figure 1

Refer to the MOSFET amplifier shown in Figure 1.

a) [5 points] How many stages are there? For each stage, identify the type of the stage, the amplifier transistor(s) and the load transistor(s).

There are three stages. The first stage is a differential stage with an active load. The amplifier transistors are Q_1 and Q_2, and the load transistors are Q_3 and Q_4. The second stage is a common-source amplifier. The amplifier transistor is Q_5 and the load transistor is Q_7.

The third stage is a common-drain (or source follower) stage. The amplifier transistor is Q_6 and the load transistor is Q_8. Transistors Q_9 and Q_{10} form a current mirror.

Assume in the following that $k'_n = 250\ \mu A/V^2$, $V_{tn} = 0.5$ V, $\lambda_n = 0.05\ V^{-1}$, $k'_p = 100\ \mu A/V^2$, $V_{tp} = -0.6$ V, and $\lambda_p = 0.1\ V^{-1}$.

Assume $I_{REF} = 100\ \mu A$, and that all MOSFETs have a (W/L) ratio equal to 20, except for of Q_5 which has $(W/L) = 40$.

<u>Neglect channel length modulation in DC analyses.</u>

b) [6 points] For each MOSFET, find the drain current and the overdrive voltage V_{OV} when $V_1 = V_2 = 0$. This condition ($V_1 = V_2 = 0$) results in $V_{OUT} = 0$. Show your results in the following format:

Transistor	Drain Current (μA)	Overdrive Voltage (V)
Q1		
Q2		
:		

Since Q_9 and Q_{10} are matched, this means that $I_{D9} = I_{D10} = 100$ uA. The current splits equally in Q_1 and Q_2 since they are matched and have the same V_{GS} (and channel length modulation is being neglected). Therefore $I_{D1} = I_{D2} = 50$ uA. $I_{D1} = I_{D3}$ and $I_{D2} = I_{D4}$ => $I_{D3} = I_{D4} = 50$ uA. The current in Q_7 is 100 uA, since it is mirroring I_{REF}. This same current flows in Q_5 => $I_{D5} = I_{D7} = 100$ uA. Same for Q_6 and Q_8: $I_{D6} = I_{D8} = 100$ uA.

V_{OV} for the various MOSFETs is calculated from

$I_D = \frac{1}{2}k'(\frac{W}{L})V_{OV}^2 \Rightarrow V_{OV} = \sqrt{\frac{2I_D}{k'(\frac{W}{L})}}$ where k' is k'_n for NMOS and k'_p for PMOS. For PMOS transistors, V_{OV} is negative. The table shown below also shows the value of V_{GS} of the transistors, and the values of g_m and r_o.

	k' (uA/V2)	W/L	VT (V)	Lambda (1/V)	ID (uA)	VOV (V)	VGS (V)	gm (mA/V)	ro (kOhm)
Q1	250	20	0.5	0.05	50	0.1414	0.6414	0.7071	400
Q2	250	20	0.5	0.05	50	0.1414	0.6414	0.7071	400
Q3	100	20	-0.6	0.1	50	-0.2236	-0.8236	0.4472	200
Q4	100	20	-0.6	0.1	50	-0.2236	-0.8236	0.4472	200
Q5	100	40	-0.6	0.1	100	-0.2236	-0.8236	0.8944	100
Q6	250	20	0.5	0.05	100	0.2	0.7	1	200
Q7	250	20	0.5	0.05	100	0.2	0.7	1	200
Q8	250	20	0.5	0.05	100	0.2	0.7	1	200
Q9	250	20	0.5	0.05	100	0.2	0.7	1	200
Q10	250	20	0.5	0.05	100	0.2	0.7	1	200

c) [4 points] Find the total power dissipation in the circuit.

The total power dissipated in the circuit comes from the two supplies.

The current in the (+2.5V) supply is equal to $I_{D3} + I_{D4} + I_{D5} + I_{D6}$ = 50 + 50 + 100 + 100 = 300 uA.
The current in the (–2.5V) supply is $I_{D9} + I_{D10} + I_{D7} + I_{D8}$ = 100 + 100 + 100 + 100 = 400 uA, into the supply.
The total power dissipation is therefore (2.5)(0.3m) + (2.5)(0.4m) = 1.75 mW.

d) [7 points] Find the differential gain $A_d = v_{out}/(v_1 - v_2)$ by calculating $v_{d2}/(v_1 - v_2)$, v_{d5}/v_{d2}, and v_{out}/v_{d5}.

The first stage gain is given by $v_{out}/(v_1 - v_2) = g_{m2}(r_{o2}//r_{o4})$ = 0.7071(200//400) = 94.28 V/V.
The second stage gain is given by $v_{d5}/v_{d2} = -g_{m5}(r_{o5}//r_{o7})$ = 0.8944(100//200) = –59.63 V/V.
The third stage gain is given by $v_{out}/v_{d5} = (g_{m6}R'_L)/(1+ g_{m6}R'_L)$ with $R'_L = (r_{o6}//r_{o8})$ = 100 K. Therefore v_{out}/v_{d5} = 100/101 = 0.99 V/V.
The overall gain is 94.28 × (-59.63) × (0.99) = –5565.7 V/V

e) [6 points] Find the common-mode gain $A_{cm} = v_{out}/v_{icm}$ when $v_1 = v_2 = v_{icm}$. What is the common-mode rejection ratio of the amplifier (in dB)?

Since $r_{o3} = r_{o4}$ and $g_{m3}r_{o3} >> 1$, the first stage common-mode gain is given by $-1/(2g_{m3}r_{o10})$ = –1/(2 × 0.4472 × 200) = –0.00559 V/V
The second and third stages have the same gain as in part (d).
The common-mode gain is therefore (–0.00559) × (–59.63) × 0.99 = 0.33 V/V
The CMRR is 20 log(5566/0.33) = 84.54 dB

f) [4 points] Find the input common-mode range by calculating the maximum and minimum values of $V_1 = V_2 = V_{ICM}$ for which all MOSFETs are saturated.

The maximum V_{ICM} is determined by Q_1 leaving SAT => $V_{DS1} = V_{OV1}$ or $V_{GD1} = V_{tn}$ => $V_{ICMmax} - V_{G3} = V_{tn}$ => $V_{ICMmax} = V_{GS3} + 2.5 + V_{tn}$ = –0.8236 + 2.5 + 0.5 = 2.1764 V
The minimum V_{ICM} is determined by Q_{10} leaving SAT => $V_{DS10} = V_{OV10}$ => $V_{S1} - (-2.5) = V_{OV10}$ => $V_{ICMmin} - V_{GS1} + 2.5 = 0.2$ => V_{ICMmin} = 0.6414 – 2.5 + 0.2 = –1.659 V

g) [2 points] Find the minimum output voltage V_{OUT} for which *all* MOSFETs remain saturated. What transistor determines this limit?

The minimum output voltage corresponds to the condition ***Q₈*** at edge of SAT => $V_{DS8} = V_{OV8}$ => $V_{OUTmin} - (-2.5) = 0.2$ => V_{OUTmin} = –2.3 V.

h) [2 points] Find the maximum output voltage V_{OUT} for which *all* MOSFETs remain saturated. What transistor determines this limit?

The maximum output voltage corresponds to the condition ***Q₅*** at edge of SAT since Q_5 enters the linear region before Q_6 does as V_{OUT} increases => $|V_{DS5}| = |V_{OV5}|$ => $2.5 - (V_{OUTmax} + V_{GS6}) = 0.2236$ => V_{OUTmax} = 2.5 – 0.7 – 0.2236 = 1.576 V

i) [4 points] A capacitor C_C is connected from the output node to the drain of Q_2. Neglecting all other capacitances in the circuit, find the frequency of the resulting zero and pole.

The zero is at G_{m2}/C_C where G_{m2} is the transconductance of the combined stage 2 – stage 3 amplifier. The pole is at a $1/(R_1R_2G_{m2}C_C)$ where R_1 is the output resistance of stage 1, and R_2 is the output resistance of stage 3.
R_1 is therefore $r_{o2}//r_{o4}$ = 133.3 KΩ
R_2 is therefore $(1/g_{m6})//r_{o6}//r_{o8}$ = 1 // 200 // 200 = 0.99 KΩ
G_{m2} is $g_{m5}(r_{o5}//r_{o7})g_{m6}$ = 0.8944(100//200)1 = 59.63 mA/V
The zero is therefore at $59.63/(2\pi C_C) = 9.49/C_C$ GHz with C_C in pF.
The pole is therefore at $1000/(133.3\ 0.99\ 59.63\ 2\pi\ Cc) = 0.0202/C_C$ MHz with C_C in pF.

Problem 2 [10 points]

For a BJT differential amplifier, the value of β for the transistors varies between 100 and 140, around a mean value of 120. The transistors are biased using a 100 μA current source.

a) [4 points] Find the input bias and the input offset currents.

The input bias current is $I_B = (I/2)/(\beta+1)$ where I is the source current. I_B is therefore (100/2)/(120+1) = 0.413 μA. The input offset current is given by $I_B\Delta\beta/\beta$ = 0.413 (40/120) = 0.138 μA.

b) [2 points] The circuit uses collector resistors, each equal to 10 KΩ, and emitter resistors, each equal to 750 Ω. Show the circuit diagram.

See figure 7.15(a) in textbook.

c) [4 points] Find the range of values for the differential input resistance.

The differential input resistance is $R_{id} = 2(\beta+1)(r_e+R_e)$, where $r_e = V_T/I_E = V_T/(I/2)$ = 25mV/50μA = 500 Ω. At β = 100, R_{id} = 2(101)(500+750) = 252.5 KΩ; at β = 140, R_{id} = 2(141)(500+750) = 352.5 KΩ. The range of values for R_{id} is therefore 252.5 to 352.5 KΩ.

Problem 3 [20 points]

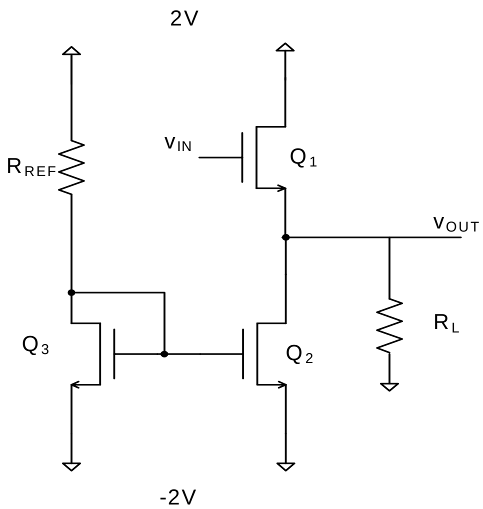


Figure 2

Refer to the circuit shown in Figure 2. The load resistor is R_L = 1000 Ω. The MOSFETs have k'_n = 200 μA/V^2 and V_{tn} = 0.5 V. The input voltage range is unrestricted.

a) [3 points] What type of output stage is this circuit?

This is a class-A output stage.

b) [10 points] Calculate the values of R_{REF} and the (W/L) ratios for the MOSFETs so that the output ranges from –0.5 to 0.5 volts with the highest efficiency and *smallest area*. All MOSFETs should be in saturation over the range of operation. Assume that Q_2 and Q_3 are matched.

The current I, flowing in R_{REF} and mirrored in Q_2, should be equal to $|V_{OUTmin}|/R_L$ = 0.5/1000 = 0.5 mA, for maximum efficiency.
Q_2 is always SAT => v_{OUT} – (–2) > V_{OV2} => V_{OV2} < v_{OUT} + 2 => V_{OV2} = –0.5 + 2 = 1.5 V, for minimum area. Therefore, $(\frac{W}{L})_2 = \frac{I_{D2}}{\frac{1}{2}k'_n V_{OV}^2}$ = 0.5m/(.1m 1.5^2)
=> $(W/L)_2$ = 2.22.
Since Q_2 and Q_3 are matched => $(W/L)_3$ = 2.22.
Since $V_{OV3} = V_{OV2}$ = 1.5V, the voltage at the drain of Q_3 is $V_{G3} = V_{GS3} - 2 = V_{OV3} + V_{tn} - 2$ = 1.5 + 0.5 – 2 = 0 V.
The voltage across R_{REF} is 2 V, therefore R_{REF} = 2V/0.5mA = 4 KΩ.
Q_1 should be saturated => $V_{OV1} = V_{DS1min} = 2 - v_{OUTmax}$ = 2 – 0.5 = 1.5 V
When $v_{OUT} = v_{OUTmax}$, $I_{D1} = I_L + I_{D2}$ = 1 mA => $(\frac{W}{L})_1 = \frac{I_{D1}}{\frac{1}{2}k'_n V_{OV1}^2}$ = 4.44.

c) [7 points] Calculate the sine wave efficiency (power_into_load / total_power) for a sine wave output with an amplitude of 0.5 V. The total_power should include the power dissipated *in all circuit elements*.

The power in the load is $P_L = \frac{V_{out\max}^2}{2R_L} = \frac{0.5^2}{2000} = 0.125\,\text{mW}$.
The power in the two supplies is 2 V (1 mA) + 2 V (1 mA) = 4 mW.
The efficiency is therefore: 0.125/4 = 3.125%

Problem 4 [30 points]

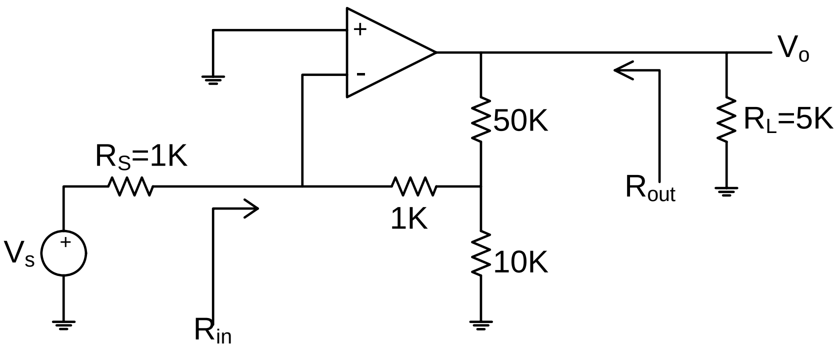


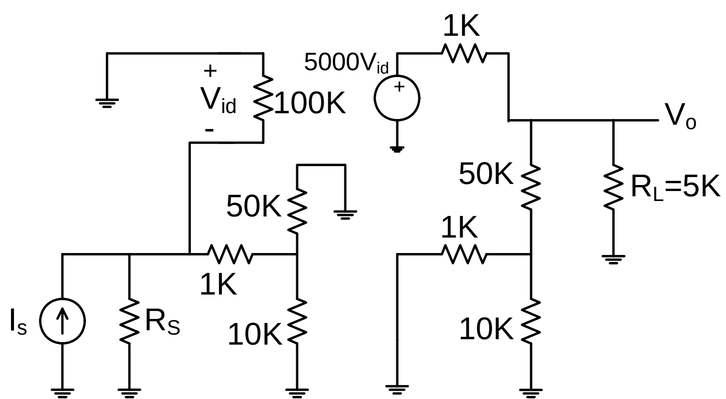
Figure 3

Consider the op-amp circuit shown in Figure 3.

a) [3 points] Determine the type of feedback used.

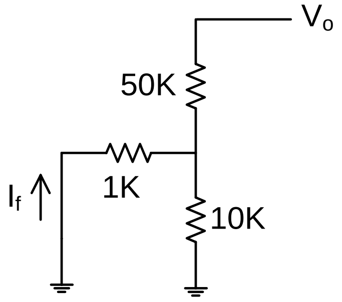
The output is a voltage that is sampled using a shunt. The input is mixed using currents, which is also a shunt. The type of feedback is therefore shunt-shunt.

b) [7 points] The op-amp is modeled by a differential input resistance R_{id} = 100 KΩ, an open-circuit voltage gain of 5000, and an output resistance of 1 KΩ. Using feedback techniques, find the open-loop gain *A*. What are the units of *A*?



The input is transformed into a current source using Norton's equivalent since the feedback is shunt-shunt.
The feedback circuit is modified (opened) to calculate the open-loop gain V_O/I_S.
From the circuit, $V_{id} = -I_S(R_S//100K//(1K+10K//50K)) = I_S(-895.14)$.
The output voltage is $V_o = 5000\ V_{id}\ R'_L/(1K + R'_L)$.
R'_L is given by 5K//(50K+1K//10K) = 4.553K.
Therefore $V_O = 4099.45\ V_{id} = 4099.45\ I_S(-895.14)$.
$A = V_o/I_S = -3669.58$ KΩ.

c) [4 points] Find the feedback factor β. What are the units of β? What is the loop gain?



The circuit to find β is shown above. The value of β is given by I_f/V_o = (1K//10K)/(1K//10K+50K)(–1/1K) = –17.857 μA/V
The loop gain is Aβ = (–3669.58 KΩ)(–17.857 μA/V) = 65.53

d) [3 points] Find the closed-loop gain A_f.

$$A_f = \frac{A}{1+\beta A} = \frac{-3669.58}{1+65.53} = -55.16\ \text{K}\Omega$$

e) [3 points] Find the voltage gain V_o/V_s.

$\frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{A_f}{R_s}$. The voltage gain is therefore V_o/V_s = –55.16 V/V.

f) [5 points] Using feedback techniques, find the input resistance R_{in}.

R_i = 1K//100K//(1K+50K//10K) = 895.14 Ω
$R_{if} = R_i/(1+\beta A)$ = 895.14/66.53 = 13.45 Ω
$R_{in} = 1/(1/R_{if} - 1/R_S)$ = 13.64 Ω

g) [5 points] Using feedback techniques, find the output resistance R_{out}.

R_o = 5K//1K//(50K+1K//10K) = 819.91 Ω
$R_{of} = R_o/(1+\beta A)$ = 819.91/66.53 = 12.324 Ω
$R_{out} = 1/(1/R_{of} - 1/R_L)$ = 12.35 Ω