

Experiment 4:

RC and RLC Circuits

In-Lab Report

A. Phase Shift Measurements

- Measure the phase shift between the input voltage and output voltage of the circuit in figure 1 using Y-T format and the X-Y format (lissajous)

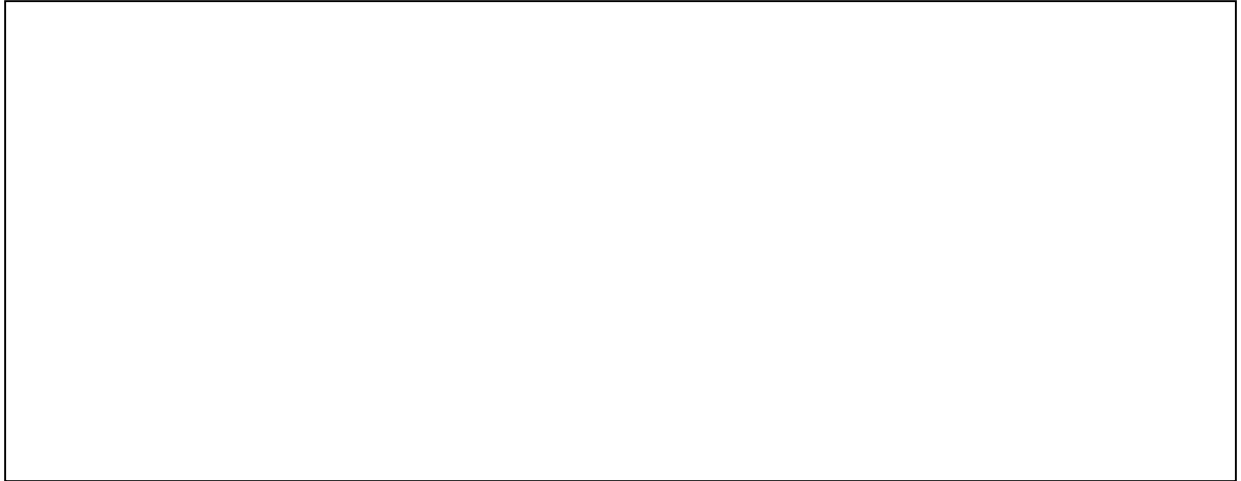
Calculated Phase Shift		
Y-T Format Δ	T=	T=
Lissajous Figure	2B=	2A=

B. Lead and Lag Networks

- Measure and draw (using Paint) the output voltage of the lag and lead networks in figure 3 and 4 if a $1 V_{pk-pk}$ Square signal is applied to the input. Below are the frequencies.

Lead Network (Measured)		
Frequency	Input Voltage	Output Voltage
100Hz	$1 V_{pk-pk}$	
1KHz	$1 V_{pk-pk}$	
10KHz	$1 V_{pk-pk}$	

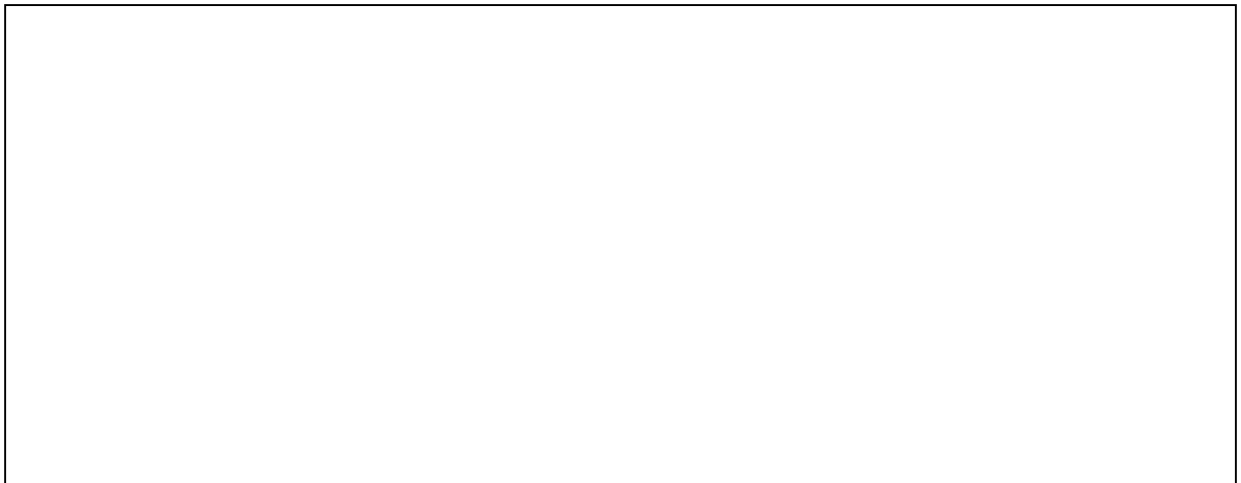
Lag Network (Measured)		
Frequency	Input Voltage	Output Voltage
100Hz	$1 V_{pk-pk}$	
1KHz	$1 V_{pk-pk}$	
10KHz	$1 V_{pk-pk}$	



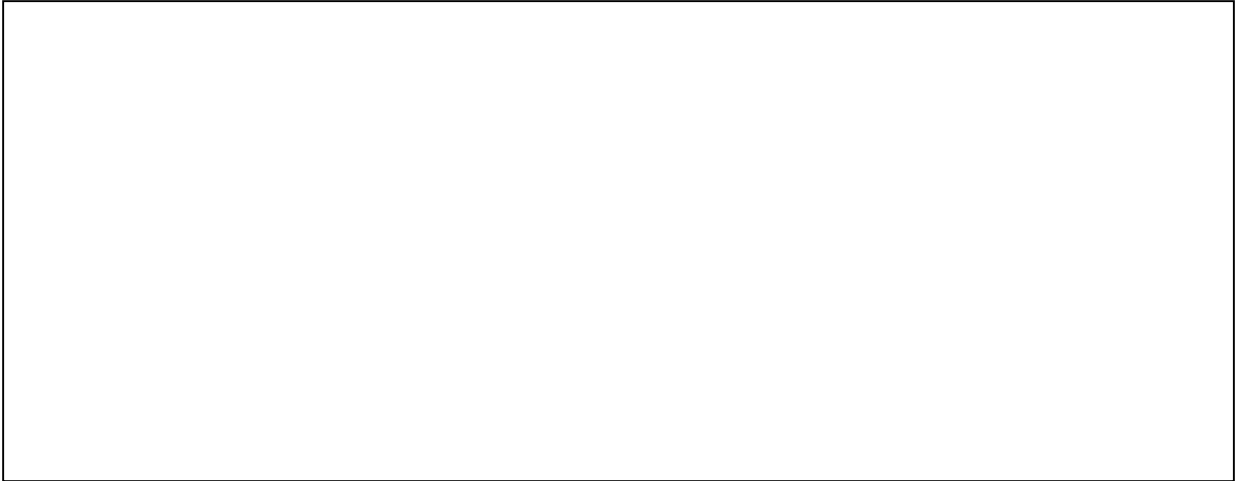
Lead 100Hz



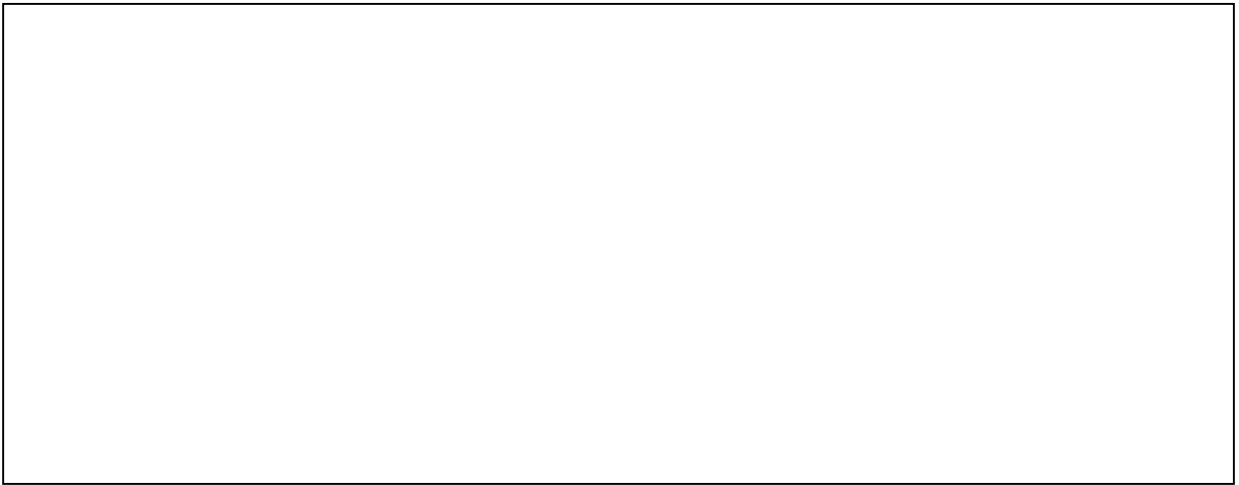
Lead 1KHz



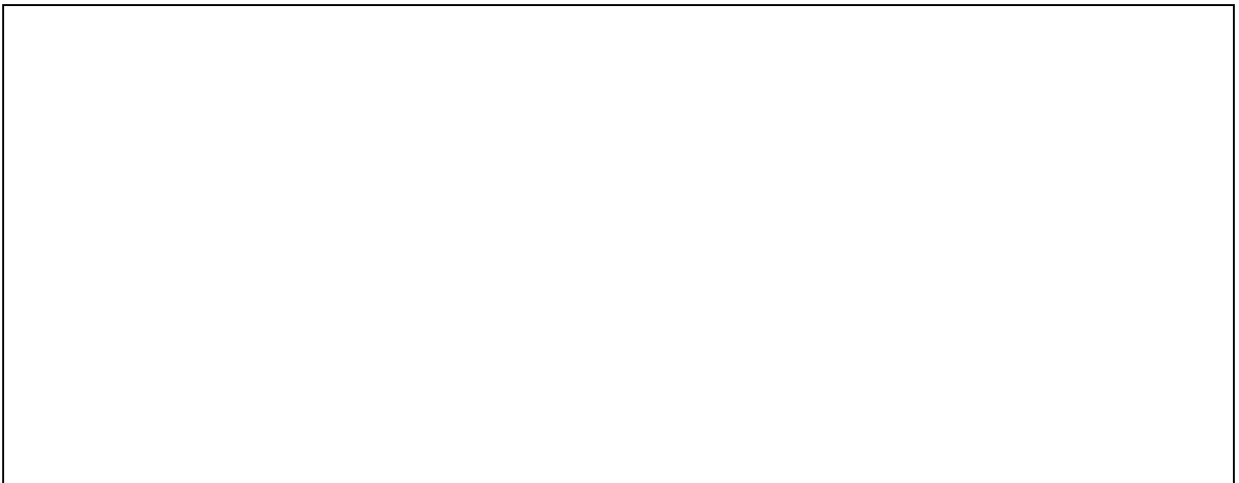
Lead 10KHz



Lag 100Hz



Lag 1KHz



Lag 10KHz

- Measure the output voltage of the lag and lead networks in figure 3 and 4 if a $1 V_{pk-pk}$ Sine signal is applied to the input. Below are the frequencies.

Lead Network (Measured)		
Frequency	Input Voltage	Output Voltage
100Hz	$1 V_{pk-pk}$	
1KHz	$1 V_{pk-pk}$	
10KHz	$1 V_{pk-pk}$	

Lag Network (Measured)		
Frequency	Input Voltage	Output Voltage
100Hz	$1 V_{pk-pk}$	
1KHz	$1 V_{pk-pk}$	
10KHz	$1 V_{pk-pk}$	

C. Series RLC circuits

- Measure the magnitude and phase angle of the output voltage for the following RLC circuits (figure 5) for an sinusoidal input voltage of 1 volt P_k-P_k

R=100Ω L=220μH C=1μF			
Frequency	$V_{IN P_k-P_k}$	$V_R P_k-P_k$	ΔT
1KHz			
1.4 KHz			
2 KHz			
2.8 KHz			
4 KHz			
5.4 KHz			
7.5 KHz			
10 KHz			
14 KHz			

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20 KHz			
28 KHz			
40 KHz			
54 KHz			
75 KHz			
100 KHz			