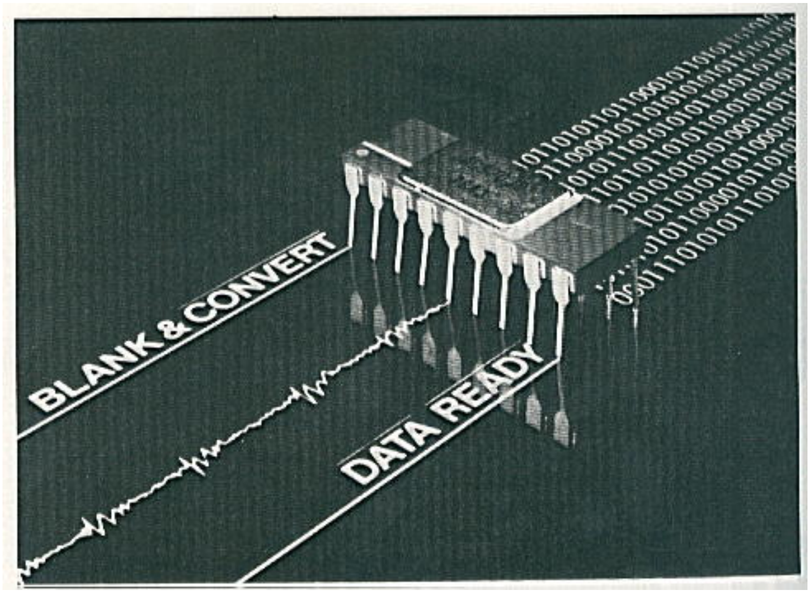
Instrumentation & Measurements
MECH 430

Chapter 7
Sampling, Digital Devices, and Data Acquisition



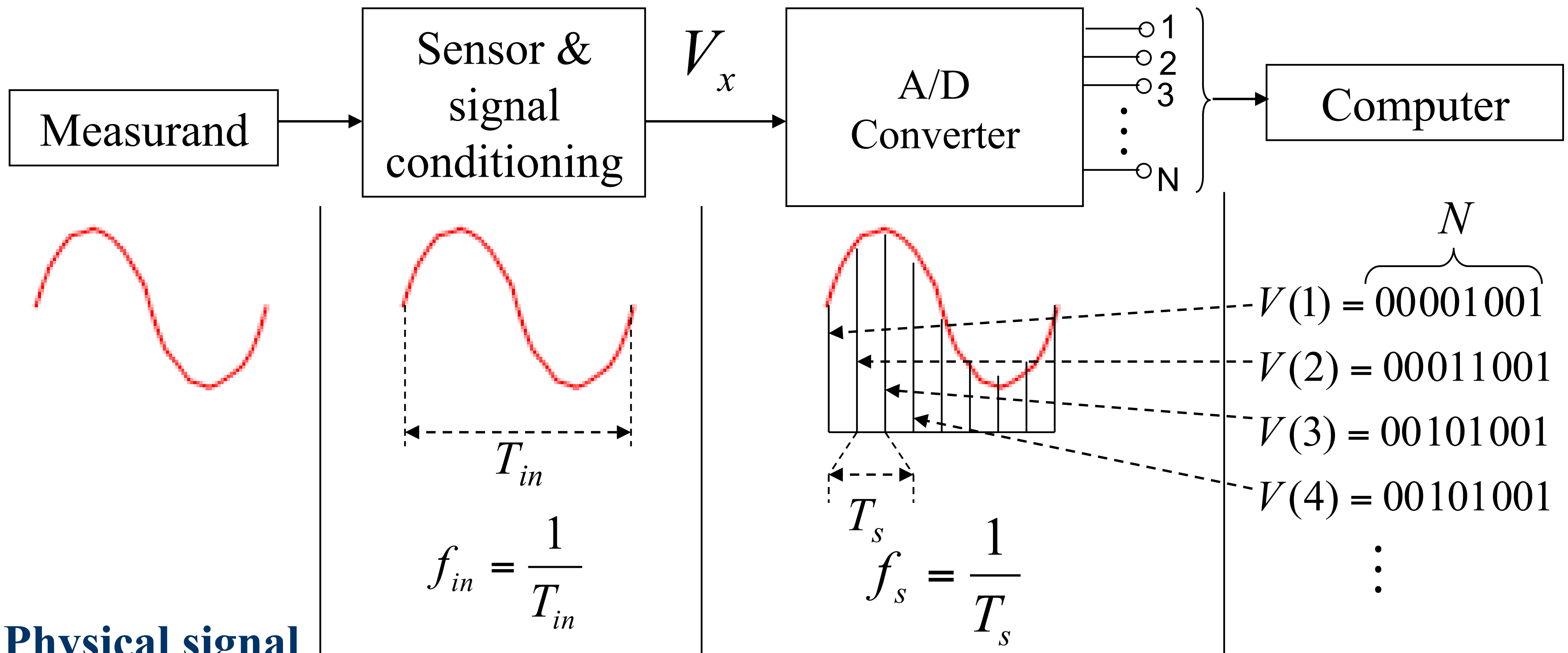
Data Acquisition

- Integrating analog electrical transducers with digital devices is cost effective and common-place.
- Digital microprocessors are central to most controllers and data-acquisitions systems today.
- How can an analog signal be represented in digital form and what are the drawbacks?
- We will discuss Analog to Digital (A2D) and Digital to Analog (D2A) devices.

Analog to Digital Conversion

- Analog to Digital (A/D) conversion involves sampling a continuous signal to deliver a discrete signal and then to subsequently digitize that discrete signal into a binary (or other) form.

Analog to Digital Conversion



Physical signal

Temperature
Pressure
Displacement
Flow,…

Electrical signal

Voltage
Current

Electrical signal conversion

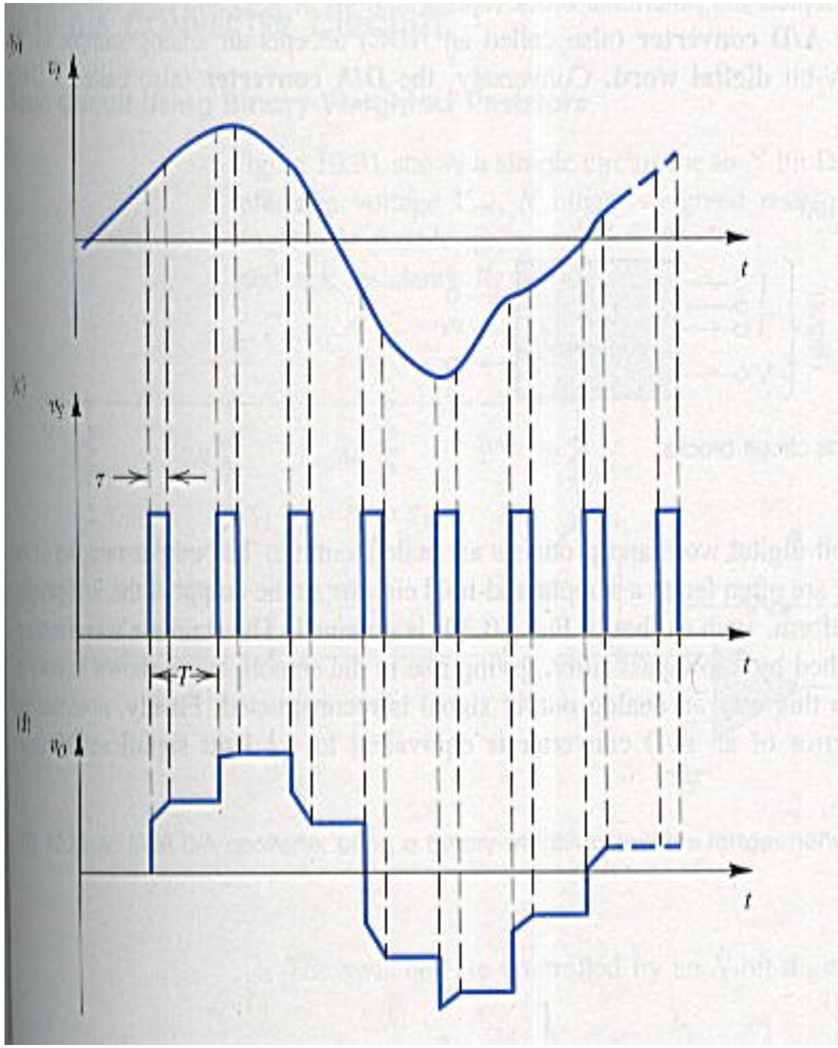
1)Sampling ($f_s > 2f_{in\_high}$) to avoid **aliasing**
2) Digitization

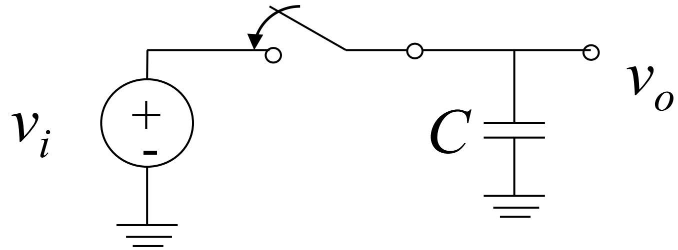
Digital signal

Sample & Hold

- Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the *conversion time*).
- An input circuit called a sample and hold performs this task—in most cases by using a capacitor to store the analogue voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input.

Sample & Hold





- The closure time τ of the switch is relatively short and the <u>samples</u> obtained are <u>stored on the capacitor</u>.
- Each of these voltages is then <u>fed to the input</u> of the ADC, which provides an N-bit binary number proportional to the value of signal sample.

Analog to Digital Conversion

- The output of an A/D converter depends on :
  - Low and high reference voltages V_{RL} and V_{RH} (If V_{RL} and V_{RH} have the same polarity, the A/D is a *unipolar* device; otherwise it is *bipolar*).
  - The number of bits k, the signal is coded into
- A k-bit A/D generates 2^k output levels called *quanta*. The minimum value is called *offset*, & the difference between the minimum and the maximum is called the *range, span* or *full scale*.
- Example, for an 8-bit code, V_{RL} will be eight zeros, V_{RH} will be eight ones and the number of levels is $2^8 = 256$.

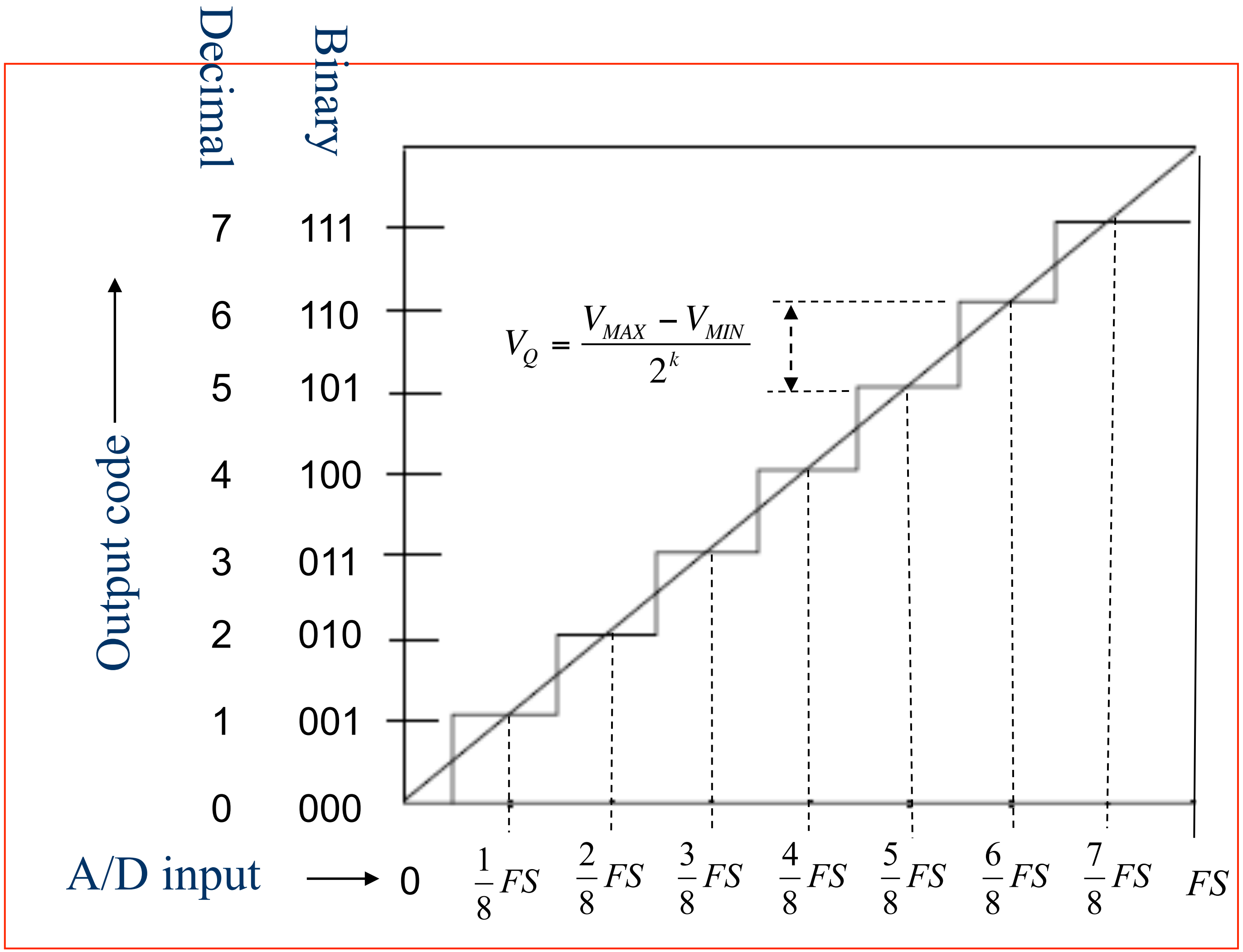
K bits Analog to Digital Converter

k = 3
3-bit ADC

Resolution:

$$V_Q = \frac{V_{MAX} - V_{MIN}}{2^k}$$

$$FS = x_{MAX} - x_{MIN}$$



Resolution

- The *resolution* of the converter indicates the number of discrete values it can produce over the range of voltage values. It is the smallest variation in the analog input signal that would cause the A/D output code to change by one level or quantum.
- It is usually expressed in bits. For example, an ADC that encodes an analog input to one of 256 discrete values (0..255) has a resolution of 8 bits since $2^8 = 256$
- Resolution can also be defined electrically, and expressed in volts. The voltage resolution of an ADC is equal to its overall voltage measurement range (FS) divided by the number of discrete values: $V_Q = \dfrac{V_{MAX} - V_{MIN}}{2^k}$

Resolution

Example 1:

Full scale measurement range = 0 to 10 volts

If ADC resolution is 12 bits: 2^{12} = 4096 quantization levels

ADC voltage resolution is: (10-0)/(4096) = 0.00244 volts = 2.44 mV

Example 2:

Full scale measurement range = -10 to +10 volts

If ADC resolution is 14 bits: 2^{14} = 16384 quantization levels

ADC voltage resolution is: (10-(-10))/(16384) = 20/16383 = 0.00122 volts = 1.22 mV

Resolution

- In practice, the resolution of the converter is limited by the signal-to-noise (SNR) ratio of the signal in question.
- If there is too much noise present in the analog input, it will be impossible to accurately resolve beyond a certain number of bits of resolution, the "Effective Number Of Bits" (ENOB).
- While the ADC will produce a result, the result is not accurate, since its lower bits are simply measuring noise.

Input-Output Mapping

- Any input voltage v_i is translated to its decimal equivalent N as:

$$\boxed{N = INT\left(\frac{2^k}{FS} \times \left[v_i - V_{RL}\right]\right)} \qquad (1)$$

$$FS = x_{MAX} - x_{MIN}$$

We will see what this is shortly

- Going the other way around, to find an analog voltage corresponding to a specific output N we use:

$$\boxed{v_i = N \times \left(\frac{FS}{2^k}\right) + V_{RL}}$$

A/D Conversion Relations

- Equation (1) can be stated as:

$$N = \frac{2^k}{FS}\left(v_i - V_{RL}\right) = \frac{v_i - V_{RL}}{V_Q}$$

- The decimal equivalent to a binary output $N = b_n \ldots b_1 b_0$

$$N = \sum_{i=0}^{n} b_i w^i \qquad \begin{cases} b_i \text{ is its bit value} \\ w_i \text{ is its weight} \end{cases}$$

- For example if $N = 10110010$:

$$N = \sum_{i=0}^{n} b_i w^i = 0\times 2^0 + 1\times 2^1 + 0\times 2^2 + 0\times 2^3 + 1\times 2^4 + 1\times 2^5 + 0\times 2^6 + 1\times 2^7 = 178$$

A/D Conversion Relations

- Now to find the voltage corresponding to a binary output N:

$$\boxed{v_i = \left(b_n \times 2^{-1} + b_{n-1} \times 2^{-2} + \cdots + b_1 \times 2^{-n} + b_0 \times 2^{-n-1}\right) \times FS + V_{RL}}$$

- For example if a unipolar 8-bit ADC with FS = 5V generates a binary code of 01001110 (78) the corresponding voltage value is.

$$v_i = (0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 0 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6} + 1 \times 2^{-7} + 0 \times 2^{-8}) \times 5 + 0 = 1.5234V$$

Example 3

	Minimum value (Offset)	Maximum value	Range (FS)
Unipolar A/D	0V	5V	5V
Bipolar A/D	-2.5V	+12.5V	15V
4-20 mA transmitters	4mA	20mA	16mA

k-bits	V_Q (%FS)	LSB voltage for FS = 5V
4	6.25	312mV
8	0.3906	19.5mV
10	0.0977	4.90mV
12	0.0244	1.20mV
14	0.00610	305µV
16	0.00153	75µV

Example 4

- Assume digitization of a unipolar signal that can change between 0 and 5 Volts into a 3 bit digital equivalent. Calculate the resolution, the number of quantized levels. (Answer: Res=0.625, Levels=8)
- Fill the table

Quanta Level	Binary Representation	Input Volt Range From	Input Volt Range To	ADC Output Voltage
7	111			
6	110			
5	101			
4	100			
3	011			
2	010			
1	001			
0	000			

- What is the maximum error that the output voltage can undertake? ()
- What will the maximum error be if we increased the number of bits to 4 in the previous example? Verify that the error decreases with increasing the number of bits. ()

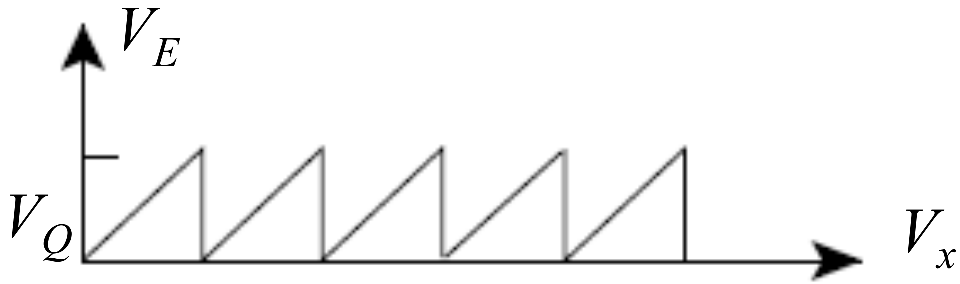
Digital to Analog Conversion

- To find the analog voltage corresponding to the a specific output N, we use: $$v_i = N \times \left(\frac{FS}{2^k}\right) + V_{RL}$$
- Analog values within a quantum level generate the same output code. The maximum error is ±½LSB (Least Significant Bit). The error V_E between the digitized voltage and the input voltage is estimated by: $V_E = v_i - NV_Q$
- The error can be lowered by increasing the number of output bits of the converter

Accuracy

- An ADC has several sources of errors:
  1) ***Quantization error*** *caused by the finite number of levels (quanta)*
  2) ***Non-linearity error*** caused by imperfections in the IC manufacturing
  3) ***Aperture error*** which is due to a clock jitter (significant at high frequencies).
- These errors are measured in a unit called the Least Significant Bit (LSB). For example, for an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%

Quantization Error



- The quantization error is the error between the analog value and its digitized representation:

$$V_E = V_X - NV_Q$$

- The minimum number of bits required in the ADC for a specific allowable error V_Q is (truncated to the next highest integer value):

$$k = \frac{\log\left(\left[V_{MAX} - V_{MIN}\right]/V_Q + 1\right)}{\log(2)}$$

Example 5

- An ADC is used to sample the output voltage of a pressure transducer. The output of the sensor is 0 Volts when the pressure is 0kPa and 10Volts when the pressure reaches 10kPa.
- If the sensor error is not to exceed 0.01kPa and assuming the input of the ADC can match the output of the sensor, select the number of ADC bits needed:

$$k = \frac{\log\left(\frac{10}{0.01} + 1\right)}{\log(2)} = 9.97 \qquad \text{Choose } k = 10\text{bits}$$

Example 6

- A temperature sensor generates an output that varies within -0.5V<V_S<+2V as the temperature varies from -50°C to 200°C. The sensor gain is 0.01V/°C. The ADC has 8bits and voltage reference -5V and +5V. Discuss the characteristics of this system.

Solution:

- The sensor voltage V_s is **matched** to the input voltage of the A/D converter by $V_x = mV_s + b$

$$\begin{aligned} -0.5m + b &= -5V \\ 2m + b &= 5V \end{aligned} \quad \Rightarrow m = 4; b = -3 \quad \Rightarrow \boxed{V_X = 4V_S - 3}$$

Example 6

- Therefore, the properties of this ADC are:

Span: $5.0-(-5.0V)=10.0V$; $200^oC-(-50^oC)=250^oC$

Step size: $10.0V/256 = 39.1mV$; $250^oC/256 = 0.98^oC$

Resolution: 39.1mV at 8-bit; 0.98 ^oC at 8-bit

- For example at $T = 50^oC$, the input of the ADC is:

$$V_X = [0.01V/^oC) \text{ x } 50^oC]\text{x}4 - 3V = -1.0V$$

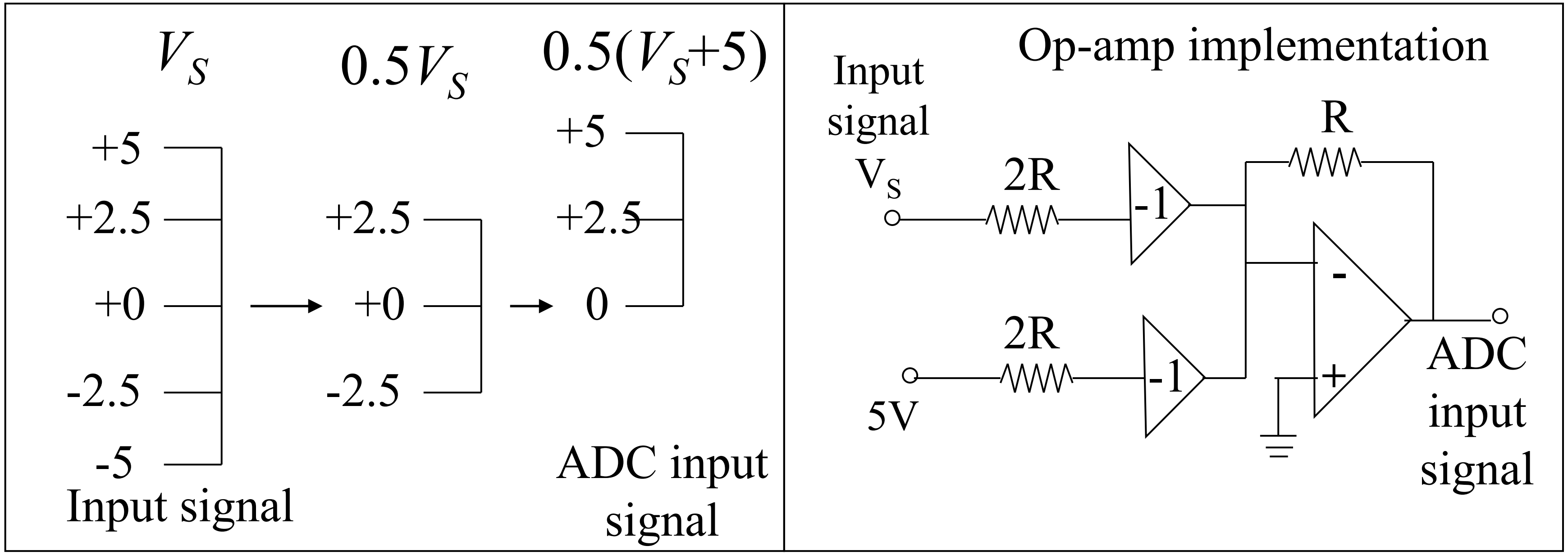
The equivalent digital output is:

Number of quantized values

$$(-1.0V-(-5V))/(0.039V) = 102 \text{ (decimal)}$$
$$= 01100110 \text{ (binary)}$$

Matching

- When connecting an input signal to an A/D converter we must take care to match the signals.
- For example adapt a bipolar signal to a unipolar ADC by scaling and adding an offset to the input:



Example 7

Given:

An IC temperature sensor with a gain of 5mV/^{o}C is used to measure the temperature of an object up to 100^{o}C. The sensor output is to be sent to an 8-bit ADC with a 0V-10V reference.

Find:

Design the required signal conditioning to interface the sensor signal to the A/D and determine the temperature resolution.

Example 7

Solution:

At 100°C, $N = 11111111$

Therefore the maximum value converted from the ADC:

$$V_X = 10\left(2^{-1} + 2^{-2} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-6} + 2^{-7} + 2^{-8}\right) = 9.9609375V$$

But we have the maximum output of the sensor is:

$$V_{S(\max)} = \left(5mV/^{o}C\right) \times 100^{o}C = 0.5V$$

And the required amplification is: $A = \dfrac{9.9609375}{0.5} = 19.92$

Example 7

- This amplification may be implemented via a non-inverting op-amp with $R_f = 18.92\text{k}\Omega$ and $R_i = 1\text{k}\Omega$

- Finally, the temperature resolution that is possible is:

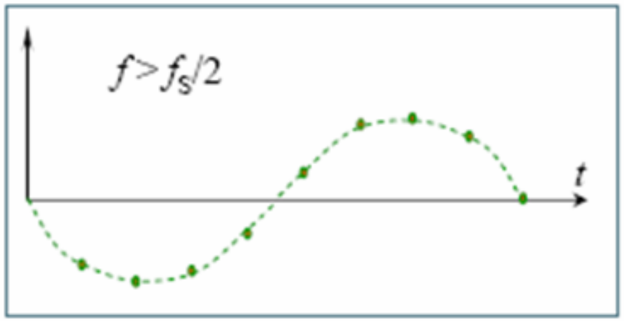
resolution

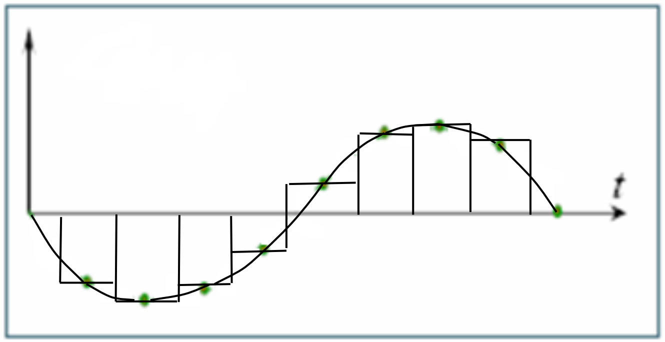
$$\Delta T = \frac{V_Q}{A}\frac{1}{5mV/^{o}C} = \frac{10/\left(2^{8}\right)}{19.92}\frac{1}{5\left(10^{-3}\right)} = 0.39^{o}C$$

amplification gain

Sampling Rate

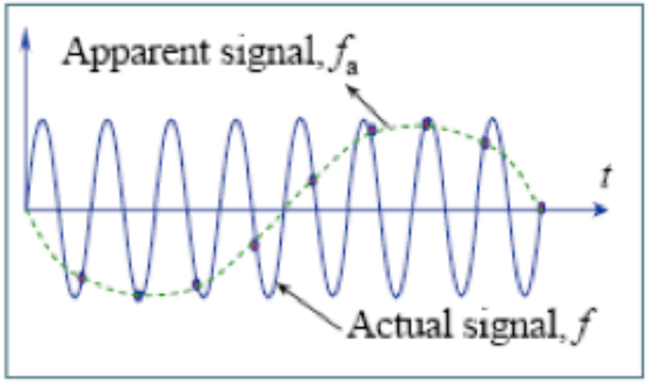
- The analog signal is continuous in time and it is necessary to convert this to a flow of digital values.
- It is therefore required to define the rate at which new digital values are sampled from the analog signal.
- The rate of new values is called the sampling rate or sampling frequency of the converter.





Sampling Rate

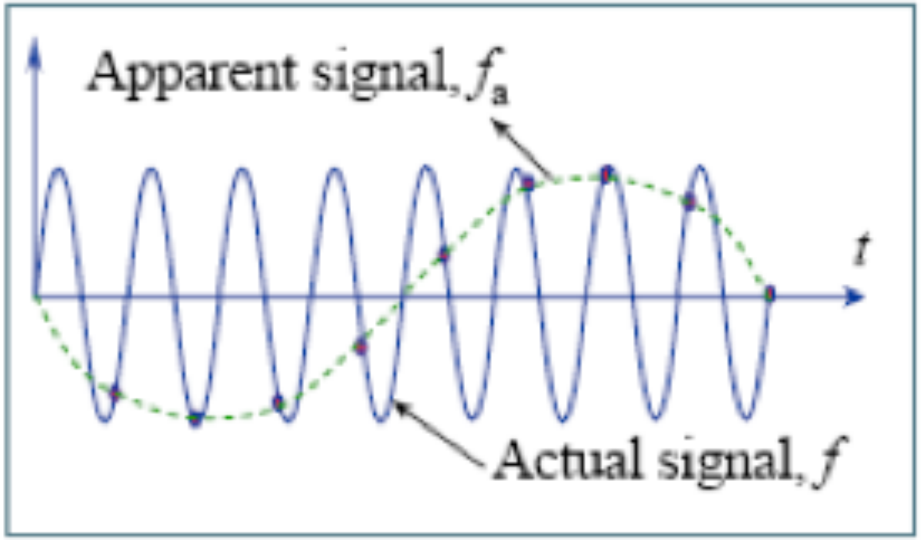
- There is no way of knowing, by looking at the output, what the input was doing between one sampling instant and the next.



- This faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the ***Shannon-Nyquist sampling theorem***.

Sampling Rate

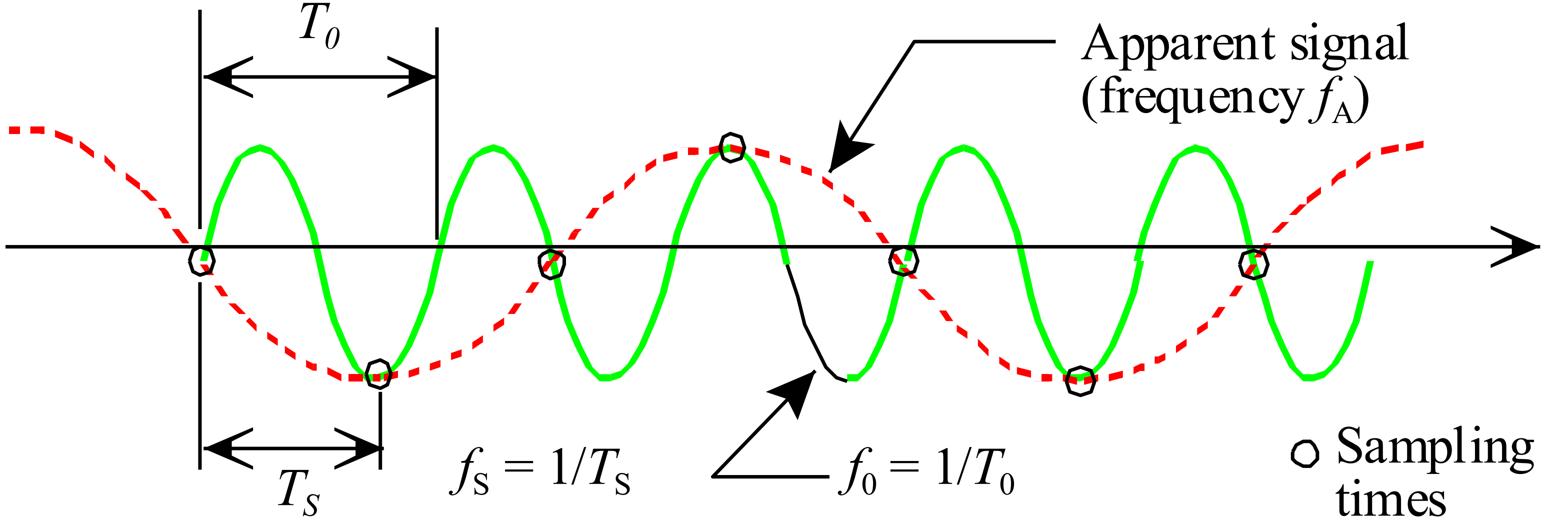
- If the input is known to be changing slowly compared to the sampling rate, then it can be assumed that the value of the signal between two sample instants was somewhere between the two sampled values.
- If, however, the input signal is changing fast compared to the sample rate, then this assumption is not valid.



Aliasing

- Aliasing is the misrepresentation of a high frequency signal as a low frequency one. This might happen when we use an ADC as shown in the figure below.
- To avoid aliasing, the sampling frequency f_s should be more than twice the highest frequency of the sampled analog signal. The sampling frequency of the analog signal f_o affects the accuracy of the discrete time representation of the signal. For a reliable approximation, the sampling frequency should be 5 to 10 times the analog signal frequency

Aliasing


T_0
Apparent signal
(frequency f_A)
T_S
$f_S = 1/T_S$
$f_0 = 1/T_0$
Sampling times

How to avoid aliasing

- To avoid aliasing make sure the sampling frequency f_s is twice the highest frequency present in the signal. This condition is known as the ***Nyquist criterion***:

$$f_s > 2f_{\max}$$

- A Rule of thumb is to have the sampling rate at least 5 to 10 times that of the highest frequency in order to accurately reproduce the waveform.