Write a VHDL code to generate a clock signal of 1Hz (50 % duty cycle) from input clock signal of 24 MHz?

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity clkdiv is
        port (clkin : in std_logic;
                reset : in std_logic;
                clkout : out std_logic );
end entity clkdiv;



architecture clkdivbeh of clkdiv is
begin
        process (clkin, reset)
        variable temp : std_logic_vector (23 downto 0);
        variable clk : std_logic;
        begin
                if (reset = '0') then
                        temp := "000000000000000000000000";
                elsif (rising_edge(clkin)) then
                        temp := temp + 1;
                        if (temp = 12000000) then
                                temp := "000000000000000000000000";
                                clk := not(clk);
                        end if;
                end if;

                clkout <= clk;
        end process;
end architecture clkdivbeh;
```