American University of Beirut
Math 255 Final Exam
Computer Architecture
Exam duration: 2 hour

Name: _____

Student number: _____

Section: Feb. 2001 - 2002

Notes:

a. Students must put this question sheet inside the answer booklet.
b. Students must use ink, however they may use pencil and ruler for drawings.
c. Students have 10 minutes reading time.

PART I: Boolean Functions representation *Each question in this part is worth 2 marks. You MUST SHOW WORKING for each question*

1. For the truth tables shown below give the representation in SOP form of the functions *P* and *Q*. Show working.

A	B	C	P
0	0	0	0
0	X	1	1
X	1	X	1
1	0	X	0

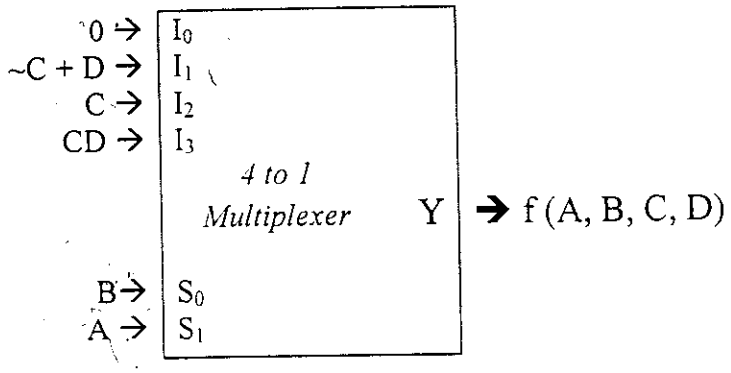
A	B	C	Q
0	0	0	0
0	1	X	1
0	X	1	1
1	0	X	0
1	1	X	1

2. What is the minterm SOP representation of the function Y = ~A ~B? Show working.

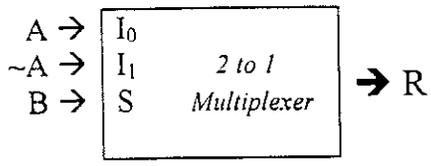
3. What is the minimal POS expression of the function represented by this K-Map?

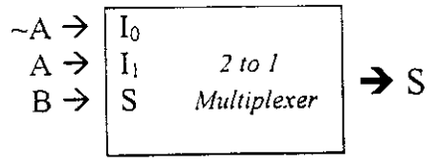
CD / AB	00	01	11	10
00	0	1	1	0
01	X	1	1	1
11	0	0	0	1
10	0	1	1	X

4. What is the expression of the function f(A, B, C, D) implemented by this circuit? Note A and B are control input (i.e. select lines). Show working.



5. Give the expressions for the functions *R* and *S* implemented by the following circuits. Note *B* is the control input (i.e. the select line).





PART II (15 marks): *Each question in this part is worth 1 mark.* DO NOT SHOW WORKING.

1. A flip flop is:

A. A device that flips its output all the time.
B. A device that can store one bit.
C. A device that can access the memory.
D. A device that can have three different output states.

2. Which one of the following is not true:

A. $X (Y + Z) = XY + XZ$
B. $\sim X \sim Y + XY = 1$
C. $X \sim X = 0$
D. $(X + YZ) = (X+Y) (X+Z)$

3. A Moore sequential circuit is a circuit:

A. With more output than input.
B. With output depending on no more than 2 previous inputs.
C. With output depending only on the present state.
D. With output depending on the present state and the current input.

4. What is the main reason for using 'virtual machine' models in computing?

A. A more accurate reflection of reality
B. Management of complexity
C. Ease of debugging
D. Simplification of hardware descriptions

5. What is the total number of states that *n* flip-flops can have?

A. n
B. 2n
C. $2^n - 1$
D. 2^n

6. Which of the following memory organisations is **NOT** POSSIBLE?

A. 10-bit address, 512 words, 64 bits per word
B. 10-bit address, 1024 words, 128 bits per word
C. 10-bit address, 16 words, 8 bits per word
D. 10-bit address, 2048 words, 16 bits per word

7. Noting that IR = Instruction Register, MBR = Memory Buffer Register, MAR = Memory Address Register, D0 = Data Register Zero, PC = Program Counter, CCR = Condition Code Register, A0 = Address Register Zero, then the fetch cycle involves the following:

A. IR, MBR, MAR, D0 and PC
B. IR, PC, MBR, and MAR
C. CCR, PC, MAR and MBR
D. A0, D0, IR and PC

8. Which of the answers is **NOT** a valid statement about the fetch/execute cycle?

A. The number of instruction bytes during the fetch sequence is fixed
B. The operation code and addressing mode information for an instruction is obtained during the fetch sequence
C. The program counter is incremented during the fetch sequence even for branch and jump instructions
D. During the execute sequence, one or more additional words containing the operands for the current instruction will always be fetched from memory

9. To convert serial data to parallel and parallel data to serial, the type of register that is needed is:

A. A universal shift register
B. A parallel load register
C. A serial input register
D. A data register

10. The storage capacity for a 256k x 64 memory chip is:

A. 1 Mbyte
B. 2 Mbyte
C. 4 Mbyte
D. 512 Kbyte

11. MOVE R1,#5 (Where R1 is a CPU register) for a Pentium CPU is a:

A. Direct addressing instruction
B. Immediate addressing type instruction
C. Stack addressing type instruction
D. Register addressing type instruction

12. The number of address bits needed in a 2 byte words addressable machine with 2048 bytes is:

A. a 2-bit address
B. an 11-bit address
C. a 10 bit address
D. None of the above

13. An appropriate combinational circuit that can be used to read a bit at a time from a serial line and convert it to a byte is

A. Multiplexer
B. Decoder
C. Demultiplexer
D. None of the above

14. Write -2789 in binary using 2's complement representation: _____

15. Write 111010101111 in decimal: _____

Part III: Sequential circuits design (12 marks).

Question 1:

a. Use clocked D flip-flops to design a 3-bit counter which counts in the sequence:

001, 011, 010, 110, 111, 101, 100, 001, ...

b. A Moore sequential network has one input and one output. When the input sequence 011 occurs, the output becomes 1 and remains 1 until the sequence 011 occurs again in which case the output returns to 0. The output then remains 0 until 011 occurs a third time, etc .

For example the input sequence: X = 0 1 0 1 1 0 1 0 1 1 0 1 0 0 1 1 1
Produces the output: Z = 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 1 1

Derive the state graph (Hint: 6 states should be enough).

Part IV: CPU architecture and Assembly language (13 marks).

Question 1: (4 marks)

Give details of the operations in Register Transfer Language of the fetch cycle and for the following assembly instructions:

```
bra #my_proc
add d0, d1
```

Question 2: (2 marks)

Give the role of each of the following CPU internal registers in one sentence:
PC, IR, CCR, D0 and A0.

Question 3: (7 marks)

Translate the following Java expression to assembly language. Use direct addressing mode assuming that d0 = a, d1 = b, d2 = c.

```
int a, b;
c = 1;
b = 2;
while ( c < 10)
{
        a = c + b;
        if ( a < 5)
        {
                c = c+ 1; b = b + 1;
        }
        c = c + 1;
}
```