American University of Beirut

CMPS 255 Final Exam

January 28, 2003

2 hour exam

Student Name: _____ Student ID: _____

Signature: _____

- *There are **ten** pages, including this one. The test is out of 100 marks, and the value of each question is provided. Please use this information to manage your time effectively.*
- *Your handwriting should be neat and readable OR I WILL NOT MARK THE ANSWER!*

Question 1:	/10
Question 2:	/10
Question 3:	/10
Question 4:	/30
Question 5:	/10
Question 6:	/10
Question 7:	/10
Question 8:	/10
	/100

Question 1: Multiple Choice [10 points]

True or false? No explanation required. Each correct answer is worth 1 points, but 1 point will be subtracted for each wrong answer, so answer only if you are reasonably certain.

1- **T** **F** The SPARC architecture is big-endian, but the Pentium is little-endian.

2- **T** **F** A big-endian file needs to be "byte swapped" before using it on a different architecture (or equivalently, the program needs to know the format of the file and work with it as appropriate for the big/little-endian format.)

3- **T** **F** Multi-byte words are stored as a sequence of bytes, in which the address of the multi-byte word is the same as the byte of the word that has the lowest address.

4- **T** **F** The "control section" of the CPU interprets instructions and effects register transfers.

5- **T** **F** The ARC datapath is made up of the register file and the ALU.

6- **T** **F** Subroutine linkage with a data link area passes parameters in registers.

7- **T** **F** Subroutine linkage with a stack passes parameters in a separate area in memory.

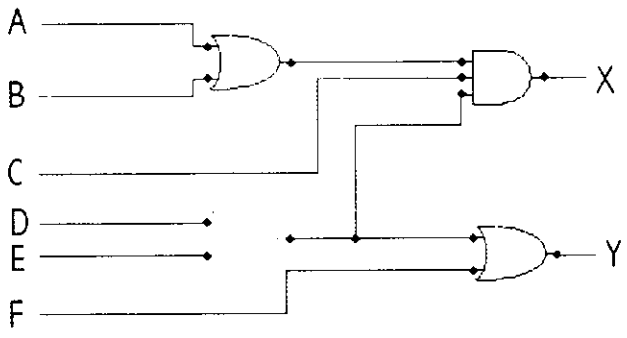
8- **T** **F** A simple register is a register that consists of flip-flops and external gates.

9- **T** **F** In general, a shift register is capable of shifting its stored bits laterally only in one direction.

10- **T** **F** Simultaneous *loading* of bits into a register is not done with a common clock pulse.

Question 2: Bubble Logic [10 points]

Convert the following logic circuit into a circuit that consists of NOR gates and inverters, using the bubble logic.

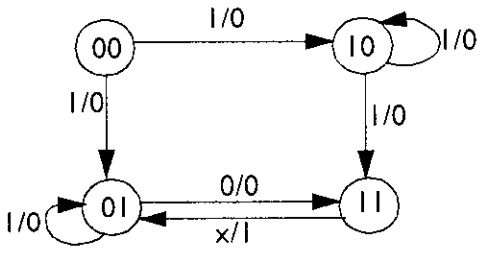


Question 3: Control Unit in SPARC CPU [10 points]

Name the five steps that the control unit carries out in executing a program, and describe ***briefly*** the role of the Decode the opcode step. (No marks will be given for naming the "decode the opcode" step)

Question 4: State Machines [30 points]

Implement the State Machine that is described by the following state diagram. You can use only D flip-flops and 4:1 multiplexers



a- Derive the state transition table. For the sake of simplifying the marking process, please follow the Q1 Q0 X, Q1+, Q0+ Z format in your table.
b- Derive the next state logic equations.
c- Draw the schematic diagram of the FSM, using D flip-flops and 4:1 multiplexers.

Question 5: Recognizing Sequences [10 points]

Give the state diagram of a Mealy type finite state machine that has one input X and two outputs Y and Z. The output Y will be 1 whenever the sequence 101 has been detected and the output Z will be 1 when the sequence 011 has been detected. These sequences can be overlapping.

The operation is illustrated in the following example:

```
X: 00110101100100111011
Y: 00000101000000000010
Z: 00010000100000010001
```

Question 6: ARC Assembly [10 points]

The Fibonacci numbers up to 200 are calculated and stored in an array. The following is the java version:

```
int[] fib = new int[20];
int a;
int b = 0;
int c = 1;
fib[0] = b;
fib[1] = c;
int i=2;
while (c<200) {
a = b;
b = c;
c = a + b;
fib[i++] = c;
}
```

Write the above code in the ARC assembly language. The table with some mnemonics and their meanings is provided below.

ld	Load a register from memory
st	Store a register into memory
sethi	Load the 22 most significant bits of a register
andcc	Bitwise logical AND
orcc	Bitwise logical OR
orncc	Bitwise logical NOR
srl	Shift right (logical)
addcc	Add
call	Call subroutine
jmpl	Jump and link (return from subroutine call)
be	Branch if equal
bneg	Branch if negative
bcs	Branch on carry
bvs	Branch on overflow
ba	Branch always

Question 7: Registers and Mux [10 points]

Implement a system for the following set of Register Transfer Operations. A set of operations needs to be executed during one clock cycle. Only one (or none) of the control signals Ca or Cb can be asserted (i.e. "1") at one time. You can draw the registers as block diagrams (no details)
Ca: R0 = R1; R2 = R1; R3 = R0
Cb: R0 = R3; R1 = R2; R3 = R2

Draw the logic diagram of the hardware implementation using registers and multiplexers.

Question 8: Address Instructions [10 points]

a) Write the following instruction using 2 and 1 address instruction set: A -= B - C
b) What is the total memory traffic for each instructio?