Fall 2004

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American University of Beirut
Faculty of Arts and Science,
Department of Computer Science

CMPS 255 final exam
Digital Design and Computer Architecture
Exam duration: 2 hours
Prof. G. Beydoun

Name: _____ **ID:** _____

a. Students must use this question sheet for their answers
b. Students can use the back side of each page for rough working

PART I *(10 marks):* *1 mark for each answer slot. Do not show working.*

a) For each of the truth tables shown below write down the function representation in SOP form.

A	B	C	P
0	X	0	1
0	1	1	1
0	1	X	1
1	X	X	0

A	B	C	Q
0	0	X	0
0	1	X	1
0	X	1	1
1	0	1	0
0	1	0	1

P = _____

Q = _____

b) The minterm SOP representation of the function Y (A, B) = ~A ~B is:

Y = _____

c) Consider the shown K-map:

CD / AB	00	01	11	10
00	0	1	1	0
01	X	1	X	1
11	0	X	X	1
10	0	1	0	0

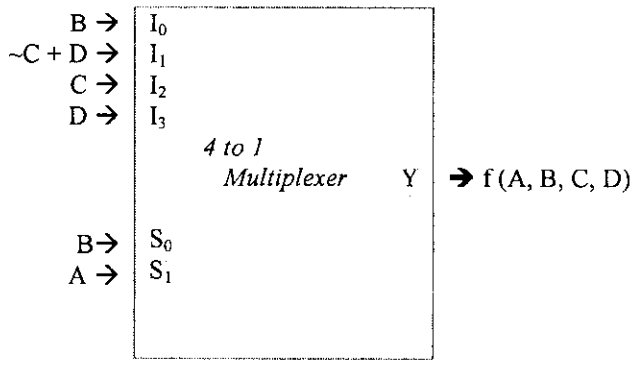
For the shown K-map, write down the following:

In minimal SOP, F = _____

In minimal POS, F = _____

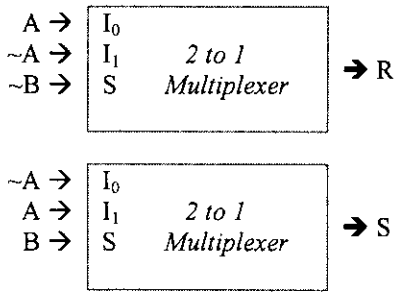
In minimal POS, ~F = _____

d) Write down the expression of the function f(A, B, C, D) implemented by the shown circuit. Note A and B are control inputs (i.e. select lines).



f = _____

e) R and S are implemented by the following circuits. Note B is the control input (i.e. the select line):



R = _____

S = _____

F (R, S) = RS + ~R ~S

Write down F in terms of A and B:

F (A, B) = _____

PART II (20 marks): *Each question in this part is worth 1 mark. Do not show working.*

1. (-29) = (_____)
2. (0110101111) = (_____)
3. Interfacing an ALU to data registers can be done with the logic macro (_____)
4. The total number of states that *n* flip-flops can have is (_____)
5. 4 registers in involved in the fetch cycle involve (_____ _____ _____ _____)
6. A device that can have three different output states is said to be (_____)
7. To convert between serial and parallel, the type of register needed is (_____)
8. Number of address bits needed in a 2 byte words addressable machine with 2048 bytes: (_____)

Answer questions 9 to 20 by ticking *True (T)* or *False (F)*:

9. The number of instruction bytes during the fetch sequence is fixed T ____ F ____
10. Memory organization: 10-bit address, 2048 words, 16 bits per word is possible T ____ F ____
11. The opcode and addressing mode for an instruction is obtained the fetch T ____ F ____
12. PC is incremented during fetch even for branch and jump instructions T ____ F ____
13. Memory organization: 10-bit address, 1024 words, 128 bits per word is not possible T ____ F ____
14. During the execute sequence, one or more additional words containing the operands for the current instruction will always be fetched from memory T ____ F ____
15. The storage capacity for a 256k x 64 memory chip is 16 KBytes T ____ F ____
16. The addressing mode for MOVE d1,#5 for a Pentium CPU is *direct* T ____ F ____
17. Memory organization: 10-bit address, 512 words, 64 bits per word is possible T ____ F ____
18. Using tri-state devices to interface internal buses in CPU to registers reduces complexity of control unit T ____ F ____
19. A Moore sequential network is a network with more output than input. T ____ F ____
20. Memory organization: 10-bit address, 16 words, 8 bits per word is not possible T ____ F ____

Part III (13 marks):

A sequential circuit has one input X and one output Z. If the input X is 1, the circuit counts in the sequence: 011, 001, 110, 010, 111, 100, 101, 011, ... If the input X is 0, the circuit counts in the sequence: 011, 110, 001, 111, 010, 101, 100, 011, ... Each time the count is 100, the circuit outputs 1.

a) Draw the state diagram of the behaviour of the circuit *(4 marks)*

b) Give the transition table of the circuit *(2 marks)*

c) Use K-maps in space provided to give excitation functions for 3 JK flipflops to implement the circuit, and output function Z. *Take J0 and K0 as the activation for the Flip Flop storing the least significant bit of the state. (7 marks).*

J0 = _____ K0 = _____

J1 = _____ K1 = _____

J2 = _____ K2 = _____

Z = _____

Part IV (8 marks):

b) *(2 marks)* The register transfer steps for *bra #my_proc* are:

d) *(6 marks)* Translate the following Java expression to assembly language. Use direct addressing mode assuming that d0 = a, d1 = b, d2 = c

```
int a = 0, b = 2, c = 1;
while ( c < (a+b) )
{
        a = c + b;
        if ( a < 5) b ++;
        c++;
}
```