American University of Beirut

CMPS 255 Final Exam

Jan. 21, 2004

2 hour exam 03:00 pm -- 05:00 pm

Student Name: _____ Student ID: _____

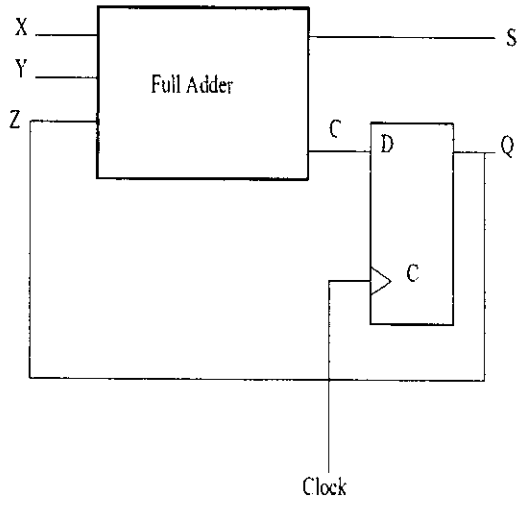
Signature: _____ Section #: _____

- *There are **TEN** pages, including this one. The test is out of 100 marks, and the value of each question is provided. Please use this information to manage your time effectively.*
- *Your handwriting should be neat and readable **OR I WILL NOT MARK THE ANSWER!***

Question 1: _____/10
Question 2 _____/15
Question 3: _____/10
Question 4: _____/10
Question 5: _____/15
Question 6: _____/15
Question 7: _____/05
Question 8: _____/05
Question 9: _____/15
Total: _____/100

Question 1: Sequential Logic Design: Analysis [10 marks]

A sequential circuit has one flip-flop Q, two inputs X, and Y, and one input S. The circuit consists of a full adder circuit connected to a D flip-flop, as shown in the figure below. Derive the state table and state diagram of the sequential circuit.



Question 2: Sequential Logic Design: Implementation [15 marks]

Design a sequential circuit with two JK flip-flops A and B and one input X. When X = 0, the state of the circuit remains the same. When X = 1, the circuit goes through the state transition from 00 to 10 to 11 to 01, back to 00, and repeats.

Question 3 State Machine Design [10 marks]

Create a state transition diagram for a machine that computes an even parity bit z for its two-bit input x_1x_0. The machine outputs a 0 when all of the previous two-bit inputs collectively have an even number of 1's, and outputs a 1 otherwise. For the initial state, assume that the machine starts with even parity.

Question 4: Memory Design [10 points]

A) How many 32 X 8 RAM chips are needed to provide a memory capacity of 1 MB

B) A program compiled for a SPARC ISA writes the 32-bit unsigned integer 0xABCDEF01 to a file and reads it back correctly. The same program compiled for a Pentium ISA also works correctly. However, when the file is transferred between machines, the program incorrectly reads the integer from the file as 0xEFCDAB. What is going wrong?

Question 5: Instruction Set Architecture [15 marks]

Using the ISA for the ARC, re-write the following Java program that takes up to 200 Fibonacci numbers and store them in an array. Explain each line for points.

```
int[] fib = new int[20];
int a;
int b = 0;
int c = 1;
fib[0] = b;
fib[1] = c;
int i=2;
while (c<200) {
  a = b;
  b = c;
  c = a + b;
  fib[i++] = c;
}
```

Mnemonic	Meaning
ld	Load a register from memory
st	Store a register into memory
sethi	Load the 22 most significant bits of a register
andcc	Bitwise logical AND
orcc	Bitwise logical OR
orncc	Bitwise logical NOR
srl	Shift right (logical)
addcc	Add
call	Call subroutine
jmpl	Jump and link (return from subroutine call)
be	Branch if equal
bneg	Branch if negative
bcs	Branch on carry
bvs	Branch on overflow
ba	Branch always

Question 6 Counters [15 marks]

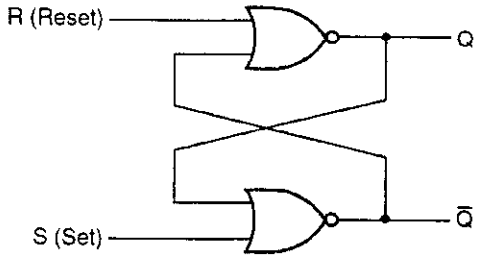
Use JK-type flip-flops to design a counter with the following repeated binary sequence: 0,1,2.

Question 7 Boolean Algebra [5 marks]

Use the properties of Boolean Algebra to prove the Demorgan's Theorem algebraically

Question 8 [5 marks]

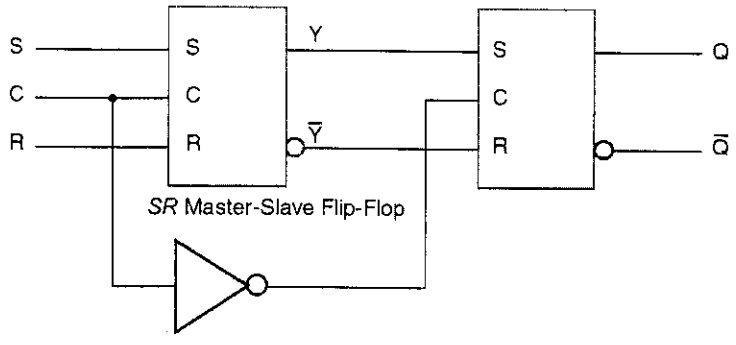
The following picture shows an S-R latch, its truth table and an S-R Master Slave Flip-flop. Can the S-R flip-flop be constructed with two cross-coupled XOR gates? Explain your answer.



(a) Logic diagram
SR Latch with NOR Gates

S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	
0	0	0	1	Reset state
1	1	0	0	Undefined

(b) Function table



SR Master-Slave Flip-Flop

Question 9: Comb. Circuit: Decoders and MuX [15 marks]

A combinational circuit is specified by the following Boolean functions:
F(A, B, C, D) = SUMm(2, 3, 6, 9, 14)
You have 3-8-line decoders with enable available. (Assume the internal structure of the decoders is based on AND gates)

A) Implement F with a decoder and external OR gates.

B) Redesign the circuit using an 8-to-1 line multiplexer.

Characteristics and Excitation Table:

Flip-Flop Characteristic Tables

(a) *JK* Flip-Flop

J	K	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}(t)$	Complement

(b) *SR* Flip-Flop

S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

(c) *D* Flip-Flop

D	$Q(t+1)$	Operation
0	0	Reset
1	1	Set

(d) *T* Flip-Flop

T	$Q(t+1)$	Operation
0	$Q(t)$	No change
1	$\overline{Q}(t)$	Complement

Flip-Flop Excitation Tables

(a) *JK* Flip-Flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) *SR* Flip-Flop

$Q(t)$	$Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(c) *D* Flip-Flop

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

(d) *T* Flip-Flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0