American University of Beirut
CMPS 255 Final Exam
Computer Architecture
Exam duration: 2 hour

ReadMe Notes:

a. I must write the answers after each question.
b. I may use any pen of any colors except red.
c. I may use the back of any page as scratch by writing SCRATCH on top of it.
d. I am NOT ALLOWED to borrow anything from other students.
e. I am NOT ALLOWED to ask any questions during the exam.
f. I am NOT ALLOWED to peek at my neighbor's paper; it is a form of cheating.
g. The instructor will be responsible for any typos not corrected during the exam.
h. Cheating of any kinds will NOT BE TOLERATED AT ALL. I should remember that trying to cheat to gain couple of points may cost me the whole semester if not more.
i. I have max 120 minutes to finish this exam which includes the time to read these notes and the questions.
j. I have checked that this Exam Booklet has 8 pages in total.

I, (NAME:_____ with student ID:_____), have read and understood the above notes

Good Luck
Prof. Eng. Mohamad Ladan

PART I:

1. What decimal value do (11010) represent in each of the following system: (3 pts)

a- Regular binary system (base 2) (ex. 101 represent 5)

b- 6-4-2-1 weighted code system

c- 5-bit word Sign and Magnitude system

d- 5-bit word 1's Complement system

c- 5-bit word 2's Complement system

2. Given $F(a, b, c, d) = \Sigma m(0, 1,4, 6, 7, 9, 11, 13, 14) + \Sigma d(2, 5, 12)$

a- Find the ***minimum*** *sum-of-products* (SOP) for F (2 pts)

b- Underline **all** the *essential prime implicants* in your above answer. (1 pt)

3- Design the following function using **one** *4-to-1 MUX,* **with *B and D as control inputs*, *and some extra* AND *and* OR *gates if needed.***

$f(A, B, C, D) = \Sigma m(0, 1, 3, 6, 7, 8, 11, 12, 14)$ (4 pts)

4. Given the following functions:

$f_1(a, b, c) = a'b + abc' + a'c$
$f_2(a, b, c) = \Sigma m(0, 1, 2, 6)$

a- Implement the above functions (f_1 and f_2)using a PLA (you only have to give the PLA diagram with the proper/correct dotted connections): (3 pts)

b- Implement the above functions (f_1 and f_2) using a ROM. (2 pts)

5- Using three clocked T flip-flops, **design** a 3-bit counter which counts in the following sequence: (3 pts)

000, 010, 100, 110, 000,.....

PART II: PLEASE Circle **the (one) best answer** for each of the following questions:
(1/2 pt each)

1. A sequential network is:

A. A switching network that has no previous inputs but remembers its previous output
B. A switching network that is the same as a combinational network
C. A switching network that has a memory device in it to remember previous inputs
D. A switching network that has a sequence of outputs and inputs with no memory

2. A flip flop is:

A. A device that flips its output all the time.
B. A device that flips its inputs all the time
C. A device that can access the memory
D. A device that can store one bit.

3. What is the total number of states that *n* flip-flops can have?

A. 2n
B. n
C. 2^n
D. 2^n-1

4. Which of the following memory organizations is **NOT** POSSIBLE?

A. 10-bit address, 512 words, 64 bits per word
B. 10-bit address, 1024 words, 128 bits per word
C. 10-bit address, 2048 words, 16 bits per word
D. 10-bit address, 16 words, 8 bits per word

5. MOV R1, A(R2) (Where R1 and R2 are CPU registers) is a:

A. Register addressing type instruction
B. Indexed addressing type instruction
C. Base-Indexed addressing type instruction
D. Both A and B

6. The number of address bits needed in a 2-byte-word (each word is 2 bytes) addressable machine with 2048 bytes is:

A. a 20-bit address
B. an 11-bit address
C. a 12 bit address
D. a 10-bit address

7. Noting that IR = Instruction Register, MBR = Memory Buffer Register, MAR = Memory Address Register, D0 = Data Register Zero, PC = Program Counter, CCR = Condition Code Register, A0 = Address Register Zero, then the fetch-decode-execute cycle involves the following:

A. IR, MBR, MAR, D0 and PC
B. IR, PC, MBR, and MAR
C. CCR, PC, MAR and MBR
D. A0, D0, IR and PC

8. A locality principle is that:
   A. Variables are mostly local in any programs
   B. Program cannot run without local variables
   C. Memory references tend to use small fraction of total memory
   D. Memory references are local to the program

9. A data path is:
   A. The path of the data on the main computer bus
   B. The buses inside the computers that carry data
   C. The ALU and its inputs and outputs
   D. It is the path between the CPU and the main memory

10. A cache hit happens when:
   A. The main memory and the hard disk are full
   B. Cache memory is used by huge numbers of computers
   C. The cache is hit by an interrupt request on the memory bus
   D. A memory word is found in the cache

Part III:

I- State whether the following statement is TRUE or FALSE. (**Every three wrongs will take away one right**) (1/2 pt each)

1- --------- A PLA is a PLD.
2- --------- Cache memory is faster than register
3- --------- Register-register operations are faster than register memory operations.
4- --------- Assembly language programs run faster than higher-level language programs.
5- --------- SRAM is faster than DRAM.
6- -------- Assembly language is just a readable representation of machine language.
7- --------- The main reason for using cache memory is that it is cheaper than main memor
8- --------- A pipeline is a mechanism of a processor-level parallelism.
9- --------- PCI bus is faster than the USB bus.
10- --------- ISA level has to do with the data path cycle in the CPU.

Part IV:

1- If you end up working in the *Silicon Valley in California* designing CPUs, you have to follow some main design principles when designing a general-purpose CPU. Give and very briefly discuss three main principles. (3 pts)

2- What is a split cache? (2 pts)

3- What is the difference between direct addressing and register addressing? (1 pt)

4- What is the key advantage of using register addressing compared to using direct addressing? (2 pts)

5- Modern CPUs use several stages pipeline in them. What is the main benefit of using the pipeline concept? What is the main effect of increasing the number of stages in a pipeline processor? (2 pts)

6- Translate the following Java expression to assembly languagc using the given IJVM instruction set. (3 pts)

```
c = 1;
b = 2;
a = c + b;
if ( a < 5)
 {
    c = c + 1;
    b = b + 1;
  }
a = a + 1;
```