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| PROF. AKKARY | DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING | | | November 19, 2010 |
|  | AMERICAN UNIVERSITY OF BEIRUT | | |  |
|  | **EECE 421 – COMPUTER Architecture** | | |  |
|  | **Quiz 1 – Fall 2010** | | |  |
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| **NAME**: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | |  |  | |
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**INSTRUCTIONS:**

* **The duration of the exam is TWO hours. No time extension.**
* **The exam is closed-book/closed-notes.**
* **Using Cell phones is not allowed in the examination room.**
* **Write your name and ID. NumBer in the space provided above.**
* **Circle only one answer.**
* **READ THE QUESTIONS CAREFULLY BEFORE ANSWERING.**
* **in some questions, more than one choice may be a valid answer. Circle the best choice you think is the most appropriate answer to the question.**
* **ALL QUESTIONS ARE EQUALLY WEIGHTED.**
* **There is no penalty for wrong answers.**
* **Use the back pages for scratch if needed**
* **Check that you have a total of 5 pages.**
* **No questions are allowed.**
* **You cannot leave the exam room for any reason until you complete the exam.**

1. Choose the one **FALSE** statement about addressing modes.

* 1. Pseudo-direct addressing, used for jumps, gets the upper 4 bits of the address from the PC.
  2. Base addressing adds an offset to a base address.
  3. Immediate addressing gets its operand from the instruction.
  4. PC relative addressing, used for branches, gets the lower 16 bit of the address from the PC.
  5. JR can jump to any address in memory.

1. Which of the following is **TRUE**?
   1. The most significant factor in computer performance is always the performance of its CPU.
   2. Decreasing response time by adding additional processors to a system almost always improves throughput.
   3. Adding processors to a computer system that uses multiple processors for separate tasks decreases the response time of a single task.
   4. Benchmarks are programs specifically chosen to debug the dapapath and control of a microprocessor.
   5. The Millions of Instructions per Second (MIPS) is the only valid metric to measure performance of a computer.
2. Total CPU power is given by: P = ½ CV2.
   1. True
   2. False
3. The relative performance of two processors with the same instruction set architecture (ISA) can be judged by clock rate.
   1. True
   2. False
4. A web server CPU is busy with computation 40% of the time and waiting for I/O 60%. Speeding up the I/O by 2 times is better for overall performance than speeding up the CPU by 3 times.
   1. True
   2. False
5. An Accumulator ISA class computer is faster than a Load-Store ISA class machine because it requires smaller number of instructions.
   1. True
   2. False
6. More than 60% of instructions in an ISA are typically used frequently in programs.
   1. True
   2. False
7. Which of the following statements about pipelining is **FALSE**:
   1. Pipelining improves performance by increasing instruction throughput.
   2. Pipelining does not decrease the execution time of an individual instruction.
   3. The ideal CPI of a pipelined processor is one.
   4. The ideal speed-up of a *k*-stage pipelined processor over a single-cycle processor is *k*.
   5. Sophisticated addressing modes that update registers can complicate hazard detection.
8. Which of the following statements about pipelining is **FALSE**:
   1. Only out-of-order issue causes out-of-order completion.
   2. Write-after-read hazards do not occur in in-order issue pipelines.
   3. Write-after-write hazards can occur in in-order issue pipelines.
   4. Optimizing compilers make write-after-write and write-after read hazards more probable.
   5. Read-after-write hazards cannot be avoided.
9. Which of the following statements is **TRUE** about the CDC computer that preformed dynamic scheduling with scoreboard:
   1. It used in-order issue and therefore did not encounter write-after-read hazards.
   2. It avoided write-after-read hazards by stalling at the decode stage.
   3. It avoided write-after-write hazards by stalling at the decode stage.
   4. It avoided read-after-write hazards by stalling at the decode stage.
   5. It avoided write-after-read hazards by enforcing in-order completion using the scoreboard.
10. Which of the following statements is **TRUE**:
    1. The reorder buffer was first used in Tomasulo’s algorithm.
    2. Most microprocessors that feature out-of-order execution use a future file.
    3. A history buffer provides better performance than a future file.
    4. Instructions write results to the reorder buffer in-order.
    5. Instructions read operands from the reorder buffer in-order.
11. Select the **TRUE** statement:

A processor uses Tomasulo’s algorithm to execute the following code segment. The latency of each operation is also shown.

Mul R1, R2, R3 (20 cycles)

Add R1, R1, R4 (1 cycle)

Ld R2, 0(R4) (3 cycles)

Sub R2, R1, R5 (1 cycle)

* 1. Issue order is Mul, Add, Ld, Sub
  2. Issue order is Add, Sub, Ld, Mul
  3. Issue order is Ld, Sub, Mul, Add
  4. Issue order is Mul, Ld, Sub, Add
  5. Issue order cannot be determined

1. Which of the following statements is **TRUE**:
   1. Tomasulo’s algorithm avoids write-after-write hazards by writing results into the register file in-order
   2. Tomasulo’s algorithm avoids write-after-write hazards by stalling at the decode stage.
   3. Tomasulo’s algorithm avoids write-after-write hazards by not writing some results into the RF.
   4. Tomasulo’s algorithm avoids write-after-write hazards by using a reorder buffer.
   5. Tomqsulo’s algorithm avoids write-after-write hazards by register renaming.
2. Which of the following statements is **TRUE**:
   1. Tomasulo’s algorithm avoids write-after-read hazards by writing results into the register file in-order
   2. Tomasulo’s algorithm avoids write-after-read hazards by stalling at the decode stage.
   3. Tomasulo’s algorithm avoids write-after-read using tag comparators in the register file.
   4. Tomasulo’s algorithm avoids write-after-read hazards by using a reorder buffer.
   5. Tomqsulo’s algorithm avoids write-after-read hazards using tag comparators in the reservation stations.
3. Which of the following statements is **TRUE**:
   1. Register windows is a fast method for reading values from different banks of registers.
   2. Register windows is effectively a hardware stack.
   3. Register windows is a compiler method for handling procedure calls and returns.
   4. Register windows is a method for executing delayed branches.
   5. Register windows is a method to avoid write-after-write hazards by using multiple banks of registers.
4. Which of the following statements is **TRUE**:
   1. A delayed branch is a branch that is delayed due to control hazards.
   2. A delayed branch causes more instructions to be flushed after a branch misprediction.
   3. A delayed branch does not require support from a compiler.
   4. A delayed branch is often followed by a useless instruction.
   5. A delayed branch is a method to maintain correct control dependences.
5. Which of the following statements is **FALSE**:
   1. Pentium Pro used reorder buffer for register renaming.
   2. Pentium Pro converted all CISC instructions to RISC using microcode sequencer.
   3. Pentium Pro was 3-wide superscalar.
   4. Pentium Pro used one centralized set of reservation stations.
   5. Pentium Pro used a BTB for branch prediction.
6. Select the **TRUE** statement:

Mul R1, R2, R3

Add R1, R1, R4

Ld R2, 0(R4)

Sub R2, R1, R5

St R1, 0(R1)

In this code there exist:

* 1. 3 RAW, 2 WAW and 2 WAR dependences
  2. 3 RAW, 4 WAW and 4 WAR dependences
  3. 4 RAW, 4 WAW and 4 WAR dependences
  4. 4 RAW, 2 WAW and 2 WAR dependences
  5. None of the above

1. A gshare predictor uses saturating counters state machines. The branch predictor state is 10 and the branch is mispredicted to be not taken. The next state will be:
   1. 00
   2. 01
   3. 10
   4. 11
   5. Need more information to determine the next state.
2. A gshare predictor uses 9 history bits and 12 address bits to index the state machines array. The size of the array is:
   1. 512 entries
   2. 1K entries
   3. 2K entries
   4. 4K entries
   5. 2M entries
3. Choose the pair of terms that are related:
   1. History buffer, bimodal predictor
   2. History buffer, gshare predictor
   3. History buffer, branch mispredictions
   4. History buffer, combined branch predictor
   5. All of the above
4. The BTB and Bimodal arrays are usually non-tagged arrays.
   1. True
   2. False
5. The only way to reduce CPI of a pipeline processor is to reduce control and data hazard stalls.
   1. True
   2. False
6. A compiler should not reorder the following instruction sequence.

BEQ R1, R0, Label

Ld R4, (R1)

* 1. True
  2. False

1. A Result Shift Register is used only for the purpose of providing precise state for exceptions.
   1. True
   2. False