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| PROF. AKKARY | DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING | | | December 10, 2010 |
|  | AMERICAN UNIVERSITY OF BEIRUT | | |  |
|  | **EECE 421 – COMPUTER Architecture** | | |  |
|  | **Quiz 2 – Fall 2010** | | |  |
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| **NAME**: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | |  |  | |
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**INSTRUCTIONS:**

* **The duration of the exam is TWO hours. No time extension.**
* **The exam is closed-book/closed-notes.**
* **Using Cell phones is not allowed in the examination room.**
* **Write your name and ID. NumBer in the space provided above.**
* **Circle only one answer.**
* **READ THE QUESTIONS CAREFULLY BEFORE ANSWERING.**
* **in some questions, more than one choice may be a valid answer. Circle the best choice you think is the most appropriate answer to the question.**
* **ALL QUESTIONS ARE EQUALLY WEIGHTED.**
* **There is no penalty for wrong answers.**
* **Use the back pages for scratch if needed**
* **Check that you have a total of 5 pages.**
* **No questions are allowed.**
* **You cannot leave the exam room for any reason until you complete the exam.**

1. Which of the following statements about pipelining is **FALSE**:
   1. Out-of-order issue causes out-of-order completion.
   2. Write-after-read hazards do not occur in in-order issue pipelines.
   3. Write-after-write hazards can occur in in-order issue pipelines.
   4. Optimizing compilers make write-after-write and write-after read hazards more probable.
   5. Read-after-write hazards can be avoided with register renaming.
2. Which of the following statements is **TRUE** about the CDC computer that preformed dynamic scheduling with scoreboard:
   1. It used in-order issue and therefore did not encounter write-after-read hazards.
   2. It avoided write-after-read hazards by stalling some writes to the register file.
   3. It performed out-of-order completion and used reorder buffer to handle branch mispredictions.
   4. It avoided read-after-write hazards by stalling at the decode stage.
   5. It avoided write-after-write hazards by enforcing in-order completion using the scoreboard.
3. Which of the following statements is **TRUE**:
   1. The reorder buffer is a buffer for instruction results.
   2. Most microprocessors that feature out-of-order execution use a future file.
   3. A history buffer provides better performance than a reorder buffer.
   4. Instructions read operands or tags from the reorder buffer in program order.
   5. Instructions write results to the reorder buffer in-order.
4. Select the **TRUE** statement:

A processor uses Tomasulo’s algorithm to execute the following code segment. The latency of each operation is also shown.

Add R1, R2, R3 (2 cycles)

Mul R1, R1, R4 (20 cycles)

Ld R2, 0(R4) (3 cycles)

Sub R2, R1, R5 (1 cycle)

* 1. Issue order is Mul, Add, Ld, Sub
  2. Issue order is Add, Sub, Ld, Mul
  3. Issue order is Ld, Sub, Mul, Add
  4. Issue order is Mul, Ld, Sub, Add
  5. None of the above

1. Which of the following statements is **TRUE**:
   1. Tomqsulo’s algorithm avoids write-after-write hazards by register renaming.
   2. Tomasulo’s algorithm avoids write-after-write hazards by stalling at the decode stage.
   3. Tomasulo’s algorithm avoids write-after-write hazards by using a reorder buffer.
   4. Tomasulo’s algorithm avoids write-after-write hazards by writing results into the register file in-order.
   5. Tomasulo’s algorithm avoids write-after-write hazards using tag matching in the RF.
2. Which of the following statements is **TRUE**:
   1. Tomasulo’s algorithm avoids write-after-read hazards by writing results into the register file in-order
   2. Tomqsulo’s algorithm avoids write-after-read hazards using tag matching in the reservation stations.
   3. Tomasulo’s algorithm avoids write-after-read hazards by stalling at the decode stage.
   4. Tomasulo’s algorithm avoids write-after-read using tag matching in the register file.
   5. Tomasulo’s algorithm avoids write-after-read hazards by using a reorder buffer.
3. Choose the one **FALSE** statement about addressing modes.

* 1. Indirect branches get the upper 4 bits of the address from the PC.
  2. Base addressing adds an offset to a base address.
  3. Immediate addressing gets its operand from the instruction.
  4. PC relative addressing uses the lower 16 bit from the PC to compute the target.
  5. Indirect branches can jump to any address in memory.

1. Which of the following is **TRUE**?
   1. The most significant factor in computer performance is always the performance of its CPU.
   2. The length of out-of-order superscalar pipeline has no impact on performance.
   3. Adding processors to a computer system that uses multiple processors for separate tasks usually increases throughput.
   4. Benchmarks are programs specifically chosen to debug the dapapath and control of a microprocessor.
   5. The Millions of Instructions per Second (MIPS) is the only valid metric to measure performance of a computer.
2. Total CPU power is given by: P = ½ CV2freq.
   1. True
   2. False
3. The relative performance of two processors with the same instruction set architecture (ISA) can be judged by the number of cycles required to execute a program.
   1. True
   2. False
4. A web server CPU is busy with computation 40% of the time and waiting for I/O 60%. Speeding up the I/O by 2 times is better for overall performance than speeding up the CPU by 4 times.
   1. True
   2. False
5. Instruction Set Architectures differ in how they access register operands, but not memory operands.
   1. True
   2. False
6. Which of the following statements about pipelining is **FALSE**:
   1. Pipelining improves performance by increasing instruction throughput.
   2. Pipelining does not decrease the execution time of an individual instruction.
   3. The ideal CPI of a pipelined processor is at most one.
   4. The ideal speed-up of a *k*-stage pipelined processor over a single-cycle processor is 1/*k*.
   5. Sophisticated addressing modes that update registers can complicate hazard detection.
7. Which of the following statements is **TRUE**:
   1. A delayed branch is a branch that is delayed due to control hazards.
   2. A delayed branch causes more instructions to be flushed after a branch misprediction.
   3. A delayed branch does not require support from a compiler.
   4. A delayed branch is a method to maintain correct control dependences.
   5. Delayed branches are less useful in superscalar processors than 1-wide processors.
8. Which of the following statements is **FALSE**:
   1. Pentium Pro performed register renaming by assigning different registers in a register alias table to instructions that write the same destination register.
   2. Pentium Pro converted all CISC instructions to RISC-like micro-ops.
   3. Pentium Pro was 3-wide superscalar.
   4. Pentium Pro used one centralized set of reservation stations.
   5. Pentium Pro used a BTB for branch prediction.
9. A gshare predictor uses saturating counters state machines. The branch predictor state is 00 and the branch is predicted to be not taken. The next state will be:
   1. 00
   2. 01
   3. 10
   4. 11
   5. Need more information to determine the next state.
10. A local correlating branch predictor uses 10 history bits and 12 address bits. The size of the state machines array is:
    1. 512 entries
    2. 1K entries
    3. 2K entries
    4. 4K entries
    5. 2M entries
11. Choose the pair of terms that are related:
    1. History buffer, bimodal predictor
    2. History buffer, gshare predictor
    3. History buffer, combined branch predictor
    4. History buffer, out-of-order execution
    5. None of the above
12. The gshare and Bimodal arrays are non-tagged arrays.
    1. True
    2. False
13. A data cache miss always causes data hazard stalls.
    1. True
    2. False
14. A compiler can safely reorder the following instruction sequence.

BEQ R1, R0, Label

Div R4, R0, R5

* 1. True
  2. False

1. A Result Shift Register can be used to provide precise state in case of exceptions.
   1. True
   2. False
2. VLIW consumes less power than superscalars because it uses less complex hardware, therefore less logic gates.
   1. True
   2. False
3. A Software pipelining does not help performance of superscalar and VLIW architectures.
   1. True
   2. False
4. A Software pipelining may not help performance of superscalar and VLIW architectures as much as loop unrolling.
   1. True
   2. False