TABLE 1. MSI snoopy cache coherence transitions due to cpu requests

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CPU Request** | **Current State** | **Hit/Miss** | **Action** | **Next State** |
| Load | Invalid | Miss | Place read for load on bus | Shared |
| Store | Invalid | Miss | Place read for store on bus | Modified |
| Load | Shared | Hit | None | Shared |
| Load | Shared | Miss | Place read for load on bus | Shared |
| Store | Shared | Hit | Place Invalidate on bus | Modified |
| Store | Shared | Miss | Place read for store on bus | Modified |
| Load | Modified | Hit | None | Modified |
| Load | Modified | Miss | Writeback,  Place read for load on bus | Shared |
| Store | Modified | Hit | None | Modified |
| Store | Modified | Miss | Writeback,  Place read for store on bus | Modified |

TABLE 2. MSI snoopy cache coherence transitions due to bus transactions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bus transaction** | **Current State** | **Hit** | **Action** | **Next State** |
| Read for load | Modified | Yes | Writeback, abort memory read | Shared |
| Read for store | Modified | Yes | Writeback, abort memory read | Invalid |
| Invalidate | Shared | Yes | None | Invalid |
| Read for load | Shared | Yes | None | Shared |
| Read for store | Shared | Yes | None | Invalid |

TABLE 3. MESI snoopy cache coherence transitions due to cpu requests

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CPU Request** | **Current State** | **Hit/Miss** | **Action** | **Next State** |
| Load | Invalid | Miss | Place read for load on bus  Other cache Hit = 1 | Shared |
| Load | Invalid | Miss | Place read for load on bus  Other cache Hit = 0 | Exclusive |
| Store | Invalid | Miss | Place read for store on bus | Modified |
| Load | Shared | Hit | None | Shared |
| Load | Shared | Miss | Place read for load on bus  Other cache Hit = 1 | Shared |
| Load | Shared | Miss | Place read for load on bus  Other cache Hit = 0 | Exclusive |
| Store | Shared | Hit | Place Invalidate on bus | Modified |
| Store | Shared | Miss | Place read for store on bus | Modified |
| Load | Exclusive | Hit | None | Exclusive |
| Store | Exclusive | Hit | None | Modified |
| Load | Exclusive | Miss | Place read for load on bus  Other cache Hit = 1 | Shared |
| Load | Exclusive | Miss | Place read for load on bus  Other cache Hit = 0 | Exclusive |
| Store | Exclusive | Miss | Place read for store on bus | Modified |
| Load | Modified | Hit | None | Modified |
| Load | Modified | Miss | Writeback,  Place read for load on bus  Other cache Hit = 1 | Shard |
| Load | Modified | Miss | Writeback,  Place read for load on bus  Other cache Hit = 0 | Exclusive |
| Store | Modified | Hit | None | Modified |
| Store | Modified | Miss | Writeback,  Place read for store on bus | Modified |

TABLE 4. MESI snoopy cache coherence transitions due to bus transactions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bus transaction** | **Current State** | **Hit** | **Action** | **Next State** |
| Read for load | Modified | Yes | Writeback, abort memory read, Hit = 1 | Shared |
| Read for store | Modified | Yes | Writeback, abort memory read, Hit = 1 | Invalid |
| Invalidate | Shared | Yes | None | Invalid |
| Read for load | Shared | Yes | Hit = 1 | Shared |
| Read for store | Shared | Yes | None | Invalid |
| Read for load | Exclusive | Yes | Hit = 1 | Shared |
| Read for store | Exclusive | Yes | None | Invalid |