1. Describe what happens in a snoopy cache coherence multiprocessor system in the following events. In your discussion, give the state transition of the involved block in both processor caches, the transaction that is sent on the external system bus, and which hardware unit supplies the data of the accessed block.

   a) A CPU write misses and the block is in exclusive-modified state in another processor.
   b) A CPU write hits a block in shared state and the block is in the cache of another processor.
   c) CPU read misses a block which is in exclusive-modified state in another processor.

Answer

a) A CPU write misses and the block is in exclusive-modified state in another processor.

The requesting processor issues a write-miss request on the external us. The request is snooped by the other processor. The other processor writes back its block and invalidates the block in its cache. The requesting processor reads the write back data from the other processor from the bus and inserts it in its cache in exclusive-modified state.

b) A CPU write hits a block in shared state and the block is in the cache of another processor.

The requesting processor sends out an invalidate request. The other processor invalidates its block. The requesting processor performs the write to its block and changes its state to exclusive-modified.

c) A CPU read misses a block which is in exclusive-modified state in another processor.

The requesting processor issues a read-miss request on the external bus. The request is snooped by the other processor. The other processor writes back the block and changes its state to Shared. The requesting processor reads the write back data from the external bus and inserts the block in its cache in Shared state. The write back data is also written to DRAM.

2. Consider the following sequence of address references issued by a CPU to a cache.

   0xFFFF0108, 0xFFFFC100, 0X1FFF7100, 0XFFFF4100, 0xFFFFC104, 0xFFFF0100, 0xFFFF4100

   a) Assuming a 2-way set associative cache with block size of 64 bytes, total capacity of 32Kbytes and LRU replacement policy. How many cache misses will occur? How many of these misses are compulsory and how many are conflict misses?
   b) Answer the same question if a 2-entry victim cache is added to the cache above.

Answer:

With a cache size of 32Kbytes and block size of 64 bytes, there is a total of 512 blocks in the cache, divided into 2 sets. Therefore the set size is 256 blocks and 8 bits are needed to index each set.
Bits 5-0 of the address are the byte offset bits, and bits 13-6 are the set index bits.
The third block address in the sequence accesses one set, and the rest of the addresses in the sequence access another set. Accounting for the tag bits, we have the following unique block accesses in this order: a1, b1, c2, d1, b1, a1, d1. (Same number here represents same set)
Without a victim cache, the first 4 accesses cause compulsory misses, the fifth access results in a hit, and the last two accesses cause conflict misses.
With a victim cache, the two conflict misses are eliminated.

(4) A data cache miss always causes data hazard stalls.

a. True
b. False

(17) A direct mapped cache is the same as a 1-way associative cache

a. True
b. False

(18) Capacity misses are inversely proportional to the number of blocks in the cache.

a. True
b. False

(20) Choose the one **TRUE** statement about write-through cache.

a. On a store miss, the store is written to memory, but only if the cache is not write-allocate.
b. On a store hit, the store is written to memory, but only if the cache is not write-allocate.
c. On a store hit, the store is written to memory, but only if the cache is write-allocate.
d. A store is written to memory regardless if the store hit or miss the cache.

(21) Conflict misses decrease as the number of blocks in the cache increase.

a. True
b. False

(22) Hardware prefetch reduces compulsory misses.

a. True
b. False

(29) A cache has a total capacity of 32K bytes. It is implemented as 4-way set associative, with block size of 32 bytes. The physical address on the machine consists of 32 bits.

Which of the following statements is **TRUE**?

a. Number of set index bits = 7 and number of tag bits = 20
b. Number of set index bits = 8 and number of tag bits = 19
c. Number of set index bits = 9 and number of tag bits = 18
d. Number of set index bits = 8 and number of tag bits = 20
e. None of the above

(30) A cache has a total capacity of 32K bytes. It is implemented as a fully set associative cache, with block size of 32 bytes. The physical address on the machine consists of 32 bits.

Which of the following statements is **TRUE**?

a. Number of tag bits = 20
b. Number of tag bits = 13
c. Number of tag bits = 27
d. Number of tag bits = 32
e. None of the above

(31) Consider the following sequence of address references issued by a CPU to a cache.

0xFFFF0108, 0xFFFFC100, 0X1FFF7100, 0XFFFF4100, 0xFFFFC104, 0xFFFF0100, 0xFFFF4100

Assuming a 2-way set associative cache with block size of 16 bytes, total capacity of 8Kbytes and LRU replacement policy. Which of these statements is **TRUE**?

a. There will be 6 compulsory misses and 1 hit
b. There will be 3 compulsory misses, 1 conflict miss and 3 hits
c. There will be 4 compulsory misses, 2 conflict misses and 1 hit
d. There will be 4 compulsory misses and hits
e. There will be 4 compulsory misses and 3 conflict misses

Solution:

4 block offset bits
512 total blocks
8 set index bits
20 tag bits

Same Blocks: A, B, C, D, B, A, D
All in same set
All will miss

(1) A direct mapped cache is the same as a 1-way associative cache

a. True
b. False

(2) Choose the one **TRUE** statement about write-through cache.

a. On a store miss, the store is written to memory, but only if the cache is not write-allocate.
b. On a store hit, the store is written to memory, but only if the cache is not write-allocate.
c. On a store hit, the store is written to memory, but only if the cache is write-allocate.
d. A store is written to memory regardless if the store hit or miss the cache.

(3) Assuming a fixed block size, Capacity misses are inversely proportional to the number of blocks in the cache.

a. True
b. False

(4) Conflict misses decrease as the number of blocks in the cache increase.

a. True
b. False

(5) Hardware prefetch reduces compulsory misses.

a. True
b. False

(6) A cache has a total capacity of 32K bytes. It is implemented as 4-way set associative, with block size of 32 bytes. The physical address on the machine consists of 32 bits.

Which of the following statements is **TRUE**?

a. Number of set index bits = 7 and number of tag bits = 20
b. Number of set index bits = 8 and number of tag bits = 19
c. Number of set index bits = 9 and number of tag bits = 18
d. Number of set index bits = 8 and number of tag bits = 20
e. None of the above

(7) A cache has a total capacity of 32K bytes. It is implemented as a fully set associative cache, with block size of 32 bytes. The physical address on the machine consists of 32 bits.

Which of the following statements is **TRUE**?

a. Number of tag bits = 20
b. Number of tag bits = 13
c. Number of tag bits = 27
d. Number of tag bits = 32
e. None of the above

(13) A CPU write hits a block in shared state and the block is in the cache of another processor. Which of the following statements is **TRUE?**

a. The other processor writes back its block and invalidates the block in its cache.
b. The other processor invalidates the block in its cache without writing the block back.
c. The other processor does nothing.
d. None of the above.

(14) A CPU write misses and the block is in exclusive-modified state in another processor. Which of the following statements is **TRUE?**

a. The other processor writes back its block and invalidates the block in its cache.
b. The other processor writes back the block and changes its state to Shared.
c. The other processor does nothing.
d. None of the above.

(15) A CPU read hits a block in shared state and the block is in the cache of another processor. Which of the following statements is **TRUE?**

a. The other processor writes back its block and invalidates the block in its cache.
b. The other processor writes back its block and invalidates the block in its cache.
c. The other processor does nothing.
d. None of the above.