FINAL EXAM
CMPS 371 Advanced Computer Architecture
February 2, 2006

Please start the answer to each question on a new page. You have 120 minutes

1. (20 points)

(a) (10 points) You are given a system with a level 1 (L1) cache, and a main memory, with the following specification:

L1 Cache cycle time: 1ns
L1 Cache hit rate: 95%
Main memory cycle time: 100ns

Compute the average memory access time

(b) (5 points) Now suppose we add a level 2 (L2) cache, so that the memory system becomes:

L1 Cache cycle time: 1ns
L1 Cache hit rate: 95%
L2 Cache cycle time: 10ns
L2 cache hit rate: 70%
Main memory cycle time: 100ns

Compute the average memory access time

(c) (10 points) Suppose we have a **single cycle** datapath with a cycle time of 5ns, and that a quarter of the instructions require a data fetch from memory. What is the speedup obtained by adding the L2 cache?

2. (30 points) Consider the 5-stage MIPS pipeline without forwarding, and with branches being resolved in the EX stage, using the ALU.

One type of hardware fault is a "stuck at fault": a register bit always produces the same value (0 or 1), regardless of the input that was previously written.

Consider the execution of the following instructions:

`lw rt, imm(rs)`
`sw rt, imm(rs)`
`add rd, rs, rt`
`beq rs, rt, imm`
`jr rs`

For each of the following failure scenarios, state which of these instructions will continue to execute correctly, and which will execute incorrectly. For the latter, explain what the effect of execution will be. Each of (a-c) is worth 10 points.

(a) The `rt` field of the IF/ID pipeline register is stuck at zero

(b) The `rt` field of the EX/MEM pipeline resigter is stuck at zero

(c) The `rs` field of the ID/EX pipeline register is stuck at zero

3. (30 points)

This question is about the tradeoffs involved in allocating die area to different functions.

Consider an instruction stream consisting only of integer and floating-point instructions. You are given 100 units of die area in which to implement integer units (ALU) and floating point units (FP). The objective is too keep all the units fully utilized. You may ignore any effects of dependencies between instructions. ALUs cannot execute floating point instrcutions, and FP's canot execute integer instructions.

For each of (a-e) below, compute the optimum numbers of ALU's and FP's to allocate so that all units are fully utilized, under the given conditions. Each part is worth 5 points.

For parts (a-c), the instruction stream contains equal numbers of integer and floating point instructions (50/50).

(a) The ALU and FP can both be implemented using 1 unit of die area. Each unit can execute an instruction in 1 cycle.

(b) An ALU can be implemented in 1 unit of area, and a FP can be implemented in 2 units of area. Each unit can execute an instruction in 1 cycle.

(c) An ALU can be implemented in 1 unit of area, and a FP can be implemented in 2 units of area. An ALU can execute an instruction in 1 cycle, and a FP can execute an instruction in 2 cycles.

Parts (d-f): repreat parts (a-c), except for an instruction stream which contains 75% integer instructions and 25% floating point instructions.

4. (20 points) Consider the MIPS pipeline **without** data forwarding. Identify all of the hazards in the program below, and for each hazard, state how many cycles are lost due to the resulting stall(s).

```
addi   $s0,   $s0,     4
lw     $s1,   0($s0)
lw     $s2,   4($s0)
add    $s3,   $s1,     $s2
```