

NOTE1: OPEN BOOK, CLOSED NOTES

NOTE2: SHOW ALL WORK IN ORDER TO RECEIVE FULL CREDIT

1. 20 pts. With A, B, and C as control inputs, realize the following four variable functions using an 8-to-1 multiplexer.

$$F = \sum_{i=1}^8 M(1, 3, 4, 7, 9, 10, 12, 13, 14, 15)$$

2. 30 pts. Design a circuit that adds 3 three bit binary numbers  $A_1A_2A_3$ ,  $B_1B_2B_3$ ,  $D_1D_2D_3$ , using half and full adders and puts out a logic one iff the decimal equivalent of the sum is divisible by  $(4)_{10}$ .

Note: Label the outputs of your adder circuit with  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$ , and  $C_{10}$  respectively as they apply

$A_1A_2A_3$   
 $B_1B_2B_3$   
 $D_1D_2D_3$

$C_{10}, S_1, S_2, S_3, S_4$

3. 30 pts. Using a PAL14L4, design a code converter that accepts as input the last five bits of the ASCII code for a hexadecimal number and outputs the corresponding 4-bit binary code. For example, if the input is 00101, the output is 1110 (E in Hex). Assume that the ASCII codes that do not represent hex digits will never occur as inputs.

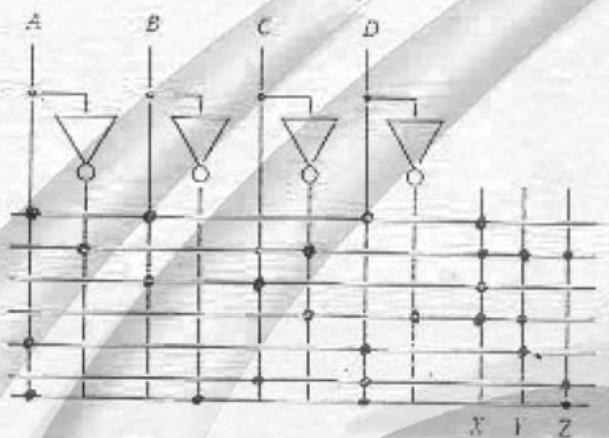
| Input<br><i>W X Y Z</i> | Hex<br>Digit: | ASCII Code for Hex Digit | ASCII Code for Hex Digit |       |       |       |       |       |       |       |       |       |       |       |
|-------------------------|---------------|--------------------------|--------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|                         |               |                          | $A_5$                    | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
| 0 0 0 0                 | 0             | 0 1                      | 1                        | 0     | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 0     | 0     |
| 0 0 0 1                 | 1             | 0 1                      | 1                        | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 0     | 1     |
| 0 0 1 0                 | 2             | 0 1                      | 1                        | 0     | 0     | 1     | 0     | 0     | 1     | 0     | 0     | 1     | 0     | 0     |
| 0 0 1 1                 | 3             | 0 1                      | 1                        | 0     | 0     | 0     | 1     | 1     | 0     | 0     | 1     | 1     | 0     | 0     |
| 0 1 0 0                 | 4             | 0 1                      | 1                        | 0     | 1     | 0     | 1     | 0     | 0     | 1     | 0     | 0     | 0     | 0     |
| 0 1 0 1                 | 5             | 0 1                      | 1                        | 0     | 1     | 0     | 1     | 0     | 1     | 0     | 1     | 0     | 1     | 0     |
| 0 1 1 0                 | 6             | 0 1                      | 1                        | 0     | 1     | 0     | 1     | 0     | 1     | 1     | 0     | 1     | 0     | 0     |
| 0 1 1 1                 | 7             | 0 1                      | 1                        | 0     | 1     | 0     | 1     | 1     | 1     | 0     | 1     | 1     | 1     | 1     |
| 1 0 0 0                 | 8             | 0 1                      | 1                        | 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 1 0 0 1                 | 9             | 0 1                      | 1                        | 1     | 1     | 0     | 0     | 0     | 1     | 0     | 0     | 1     | 0     | 1     |
| 1 0 1 0                 | A             | 1 0                      | 0                        | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 0     | 1     | 1     |
| 1 0 1 1                 | B             | 1 0                      | 0                        | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 0     | 0     |
| 1 1 0 0                 | C             | 1 0                      | 0                        | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 0     | 0     |
| 1 1 0 1                 | D             | 1 0                      | 0                        | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 0     | 0     | 0     |
| 1 1 1 0                 | E             | 1 0                      | 0                        | 0     | 0     | 1     | 0     | 0     | 1     | 0     | 1     | 0     | 0     | 1     |
| 1 1 1 1                 | F             | 1 0                      | 0                        | 0     | 1     | 0     | 0     | 1     | 0     | 1     | 0     | 0     | 0     | 0     |

4. 20 pts. The PLA below will be used to implement the following equations.

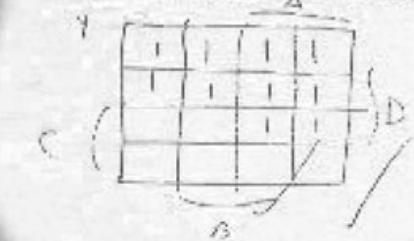
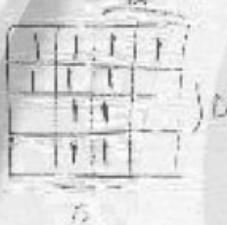
$$X = ABD + A'C' + BC + CD'$$

$$Y = A'C + AD + CD'$$

$$Z = CD + A'C' + AB'D$$



- a) Indicate the connections that will be made to program the PLA to implement these equations.  
 b) Specify the truth table for a ROM which realizes these same equations.



| A | B | C | D | X | Y | Z |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |