

Question 1. (10 points)

Encircle your answers of the following questions: (1 point each)

N.O.A = None Of the Above

1- To build a 64:1 Multiplexer from 4:1 multiplexers, you would need

- a) 17 4:1 Multiplexers
- b) 20 4:1 Multiplexers
- c) 16 4:1 Multiplexers
- d) 20 4:1 Multiplexers
- e) N.O.A

2- A static 1-Hazard causes an output that should stay at 0 to go high for a short time.

- a) F
- b) T

3- A ROM can be viewed as a programmable AND/OR array in which the AND plane is programmed as a full decoder.

- a) F
- b) T

4- The PAL circuit is used as a

- a) programmable AND, programmable OR
- b) fixed AND, programmable OR
- c) programmable AND, programmable OR
- d) fixed AND, fixed OR
- e) N.O.A

5- 2-level AND-OR circuits, can be implemented using 2-level XOR-XOR circuits:

- a) F
- b) T

6- Referring to the figure 1, when the display is '1' and C='0', what are A and B

- a) A=B='X'
- b) A=B='0'
- c) A=B='1'
- d) A=B='Z'
- e) N.O.A

7- Referring to the figure 1, IF A='Z', B='0' and C='0', the output display is

- a) 'X'
- b) '0'
- c) '1'
- d) 'Z'
- e) N.O.A

8- If the result $F = A \text{ AND } B$ is equal 1010 and $B = 1011$, so A is equal to

- a) 1100
- b) 1010
- c) 1011
- d) 0101
- e) N.O.A

9- Referring to the figure 1, the display is '0' and $A=C='1'$, $B='0'$. If the output of G1 is 1 and output of G2 is 0, which gate do you suspect is out of order?

- a) G1
- b) G2
- c) G3
- d) No enough data

10- An active HIGH S-R latch is implemented using only 2

- a) NAND gates
- b) NOR gates
- c) AND gates
- d) OR gates

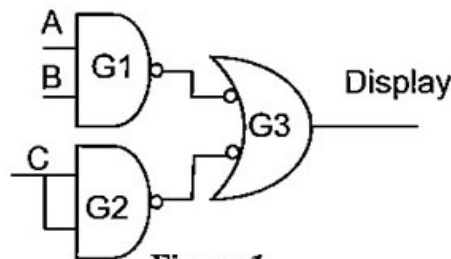


Figure 1

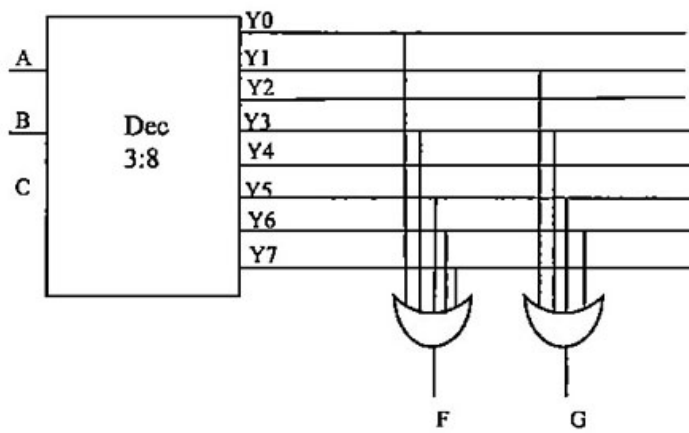
Question 2. (10 points)

Consider the following functions

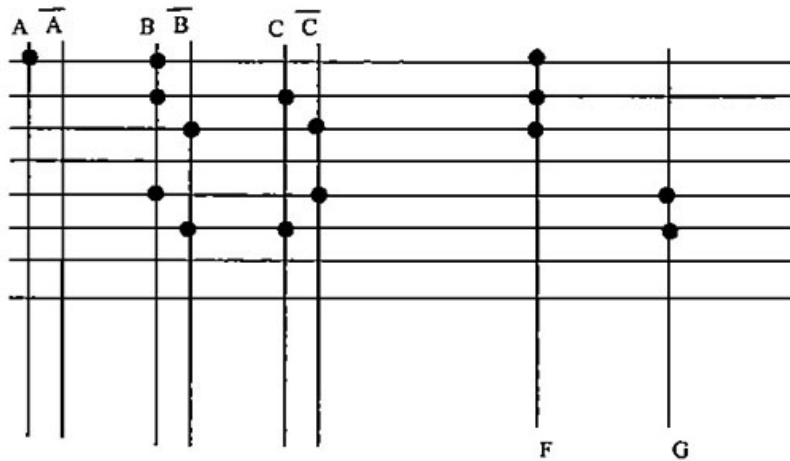
$$F(A,B,C) = AB + BC + B'C' = \sum m(0,3,4,6,7)$$

$$G(A,B,C) = BC' + B'C = \sum m(1,2,5,6)$$

1) Implement F and G using a ROM. (5 points)

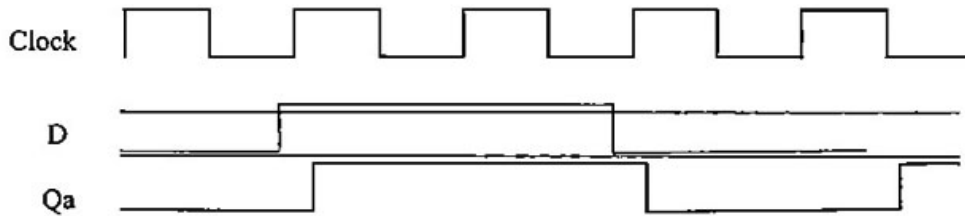


2) Implement F and G using a PLA. (5 points)

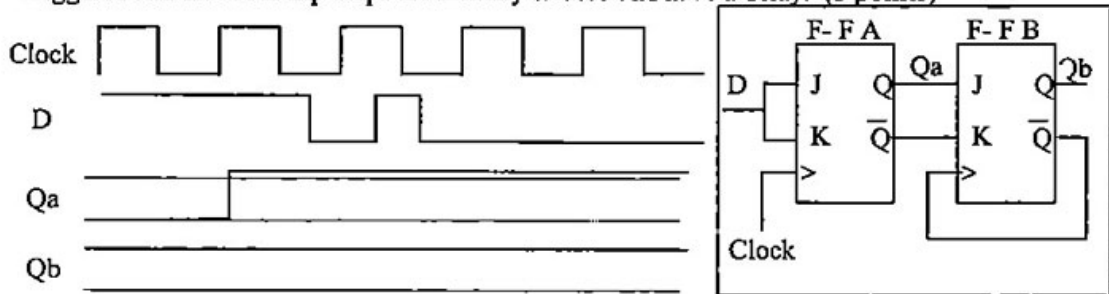


Question 3. (20 points)

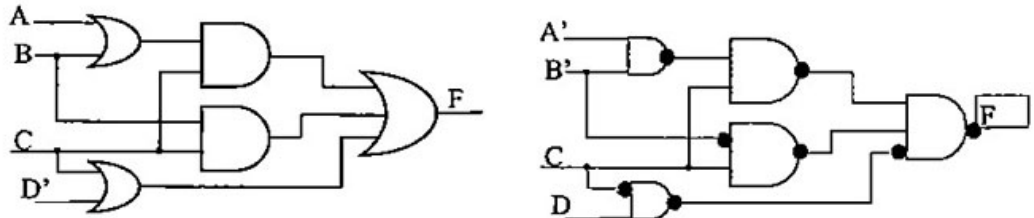
a) Draw the D input for a D flip-flop with Qa and Clock as shown: (Assume positive edge triggering and Q initially LOW) (5 points)



b) Referring to following figure, draw Qa and Qb. Assume that J-K flip-flops are edge-triggered and that both flip-flops are initially cleared and have a delay. (5 points)



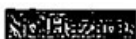
c) Convert the following circuit to NAND gates: (2.5 points)



d) Complete the timing diagram of the following function: $Y = (A' + B)(A + C)$ (5 points)

Assume that $B=C=0$, the inverter delay is 3 ms and Or delay is 5 ns.

Propose ONE solution to remove any existing hazard (glitch) of Y. (2.5 points)



Question 4 (10 points)

Design a circuit for a traffic light decoder, there are only four possible input states, represented by the binary numbers 00 through 11. These states control a traffic light on a main and side street. Each light has three outputs: Red, Yellow and Green.

If the input state is $A = B = 0$, the desired output is for the green light to be ON for the main street and the red light to be ON for the side street. (A logic 0 causes a light to be ON). The remaining outputs for each state are listed in the truth table.

Complete the design for the circuit implementation of the truth table; you can add NORs gate and Inverters.

(Note: we use a Demultiplexer for this design. The DEMUX algorithm is:

If $B=A=0$ then $Y_0 = G_1; Y_1 = Y_2 = Y_3 = 0$;

Else If $B=0$ and $A=1$ then $Y_1 = G_1; Y_0 = Y_2 = Y_3 = 0$;

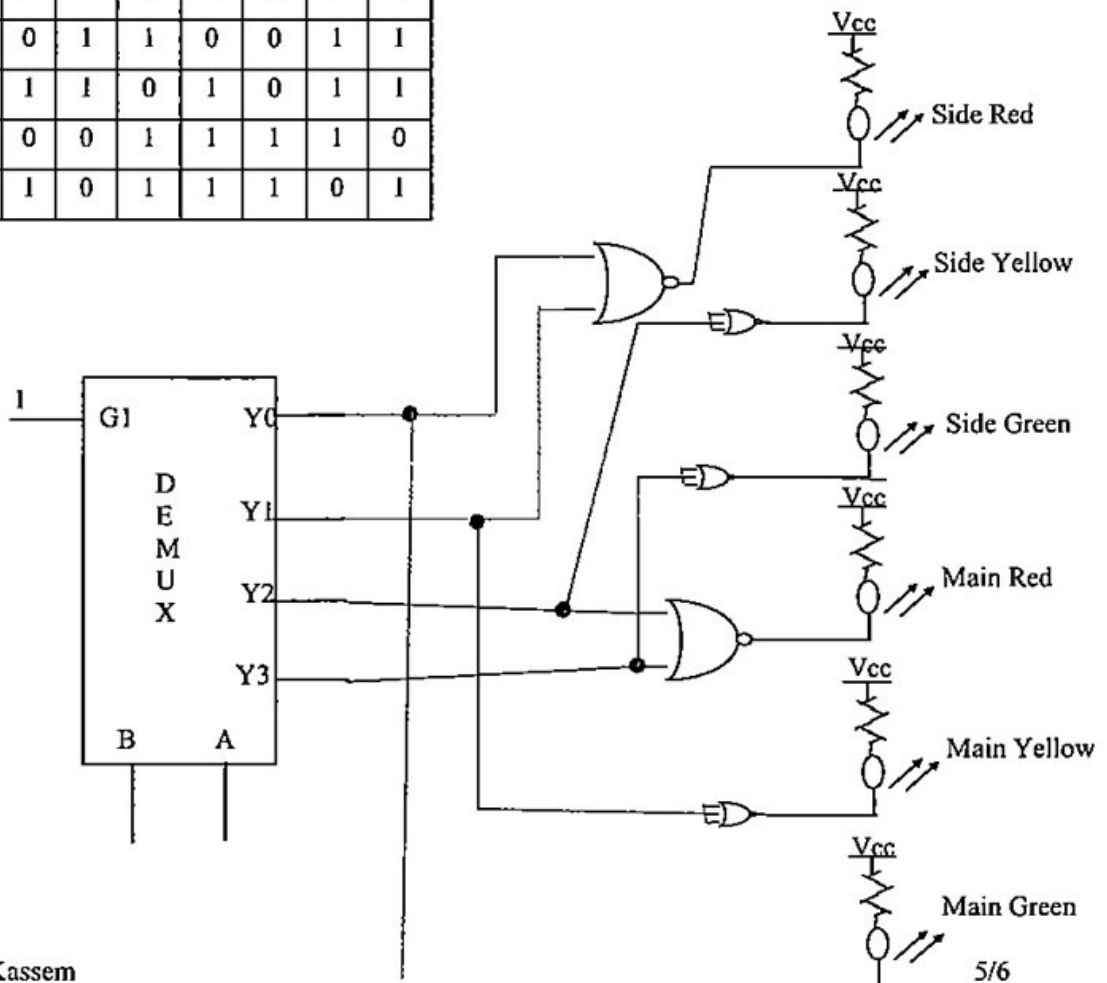
Else If $B=1$ and $A=0$ then $Y_2 = G_1; Y_0 = Y_1 = Y_3 = 0$;

Else If $B=A=1$ then $Y_3 = G_1; Y_0 = Y_1 = Y_2 = 0$;

End If)

Inputs (State)		Outputs					
B	A	Main			Side		
B	A	R	Y	G	R	Y	G
0	0	1	1	0	0	1	1
0	1	1	0	1	0	1	1
1	0	0	1	1	1	1	0
1	1	0	1	1	1	0	1

Note: R = Red, Y= Yellow and G = Green.



Question 5. (Bonus: 5 points)

Complete the timing diagram of the following circuit:

