**Question 1.** (7 points)

Encircle your answers of the following questions: (0.7 point each)

| T= True; | F= False | & | N.O.A = None Of the Above |
|---|---|---|---|

1- A register is mainly used for shifting and storing data

a) F b) T

2- A ROM can be viewed as a programmable AND/OR array in which the AND plane is programmed as a full decoder.

a) F b) T

3- Assume that, an active LOW SR flip-flop is used; the output Q is equal to 0 when R=1 and S=0.

a) F b) T

4- How many flip-flops are required to count up to $100_{10}$

a) 7 b) 10 c) 5 d) 20 e) N.O.A

5- The output in Mealy Machine is changed only when the clock edge-triggering has occurred.

a) F b) T

6- If a 50 MHz frequency is applied to the input CLOCK of a JK flip-flop with J=K=1, what will the frequency be at the output Q?

a) 50 MHz b) 25MHz c) 12.5 MHz d) 100 MHz e) N.O.A

7- Sequential circuits contain memory and combinational circuits do not.

a) F b) T

8- When a J-K flip-flop is constructed from SR flip-flop, which one of the following is true?

a) S= J.Q and R= K+J.Q' b) S= J and R= K + Q'

c) S= J.Q and R= K.Q' d) S= J.Q' and R= K.Q e) N.O.A

9- An asynchronous circuit doesn't need a CLOCK

a) F b) T

10- A J-K flip-flop is implemented using only

a) AND gates b) OR gates c) NAND gates d) NOR gates

**Question 2. (7 points)**

Design a combinational circuit that can realize the following algorithm, using only (two or three) 2:1 Multiplexers, two Full Adders, and two inverters; VCC (5 V) and GND (0V) can be used in this design.

```
Begin (algo.)
        IF Sel = 1 then
                Out = A+B
        Else
                Out = A-B
End (Algo.)
```

Note: A, B and Out are 2 bits each.

**Question 3. (7 points)**

A certain country is ruled by family of four members, **A, B, C** and **D**. **A** has 25 votes, **B** has 40 votes **C** has 15 votes and **D** has 10 votes. Any decision taken by the family is based on its receiving at least 60% of the total number of votes. Design a combinational circuit that will produce on output of 1 if a certain motion is approved by the family.

| Input | | | | Output |
|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **Decision** |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

**Question 4. (7 points)**

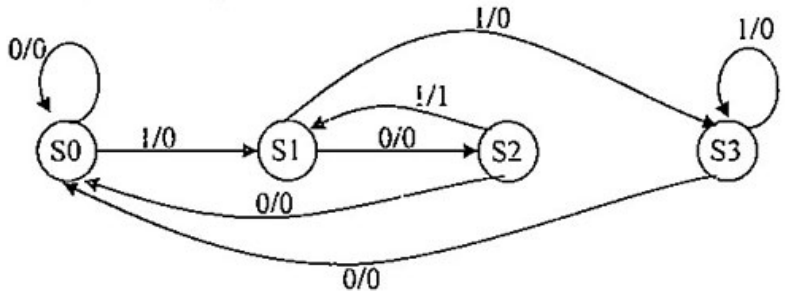
Show how to modify the internal circuit of the shift register (seen in class and home work), to load, or rotate left/right according to the following table.
*Hint: This shift register is composed of 4 MUXs and 4 D Flip-Flops.*

| Input | | Next State | | | | Action |
|---|---|---|---|---|---|---|
| A | B | Q3+ | Q2+ | Q1+ | Q0+ | |
| 0 | 0 | Q3 | Q2 | Q1 | Q0 | No change |
| 0 | 1 | Q0 | Q3 | Q2 | Q1 | Rotate Right |
| 1 | 0 | Q2 | Q1 | Q0 | Q3 | Rotate left |
| 1 | 1 | D3 | D2 | D1 | D0 | Load |

**Question 5. (7 points)**

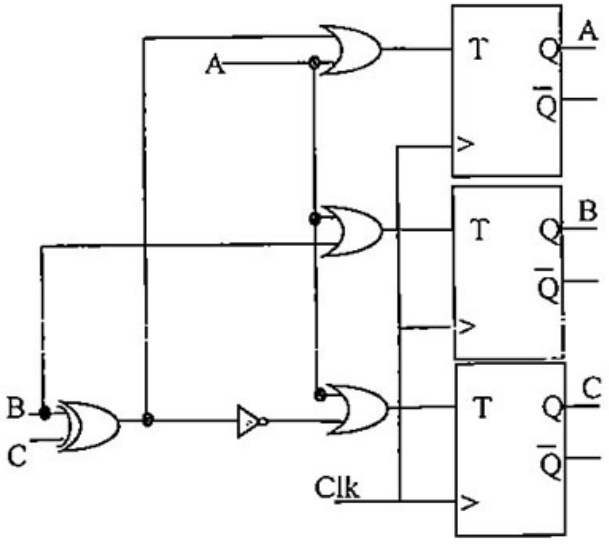
Referring to following state diagram, construct the state table and design the circuit using D flip-flops. Is it a Moore or Mealy machine? What does this design detect?
*Hint: find the next state expression for each input.*

S0=00
S1=01
S2=10
S3=11



**Question 6** (7 points)

Draw the sequence(s) of the following circuit (counter). Assume that T flip-flops are rising edge-triggered and that all flip-flops are initially cleared and have delays. Show all calculations to receive full credits.




| C | B | A | $C^+$ | $B^+$ | $A^+$ |
|---|---|---|---|---|---|
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

Use k-map if needed

| | 0 | 1 |
|---|---|---|
| 00 | | |
| 01 | | |
| 11 | | |
| 10 | | |

| | 0 | 1 |
|---|---|---|
| 00 | | |
| 01 | | |
| 11 | | |
| 10 | | |

| | 0 | 1 |
|---|---|---|
| 00 | | |
| 01 | | |
| 11 | | |
| 10 | | |

| | 0 | 1 |
|---|---|---|
| 00 | | |
| 01 | | |
| 11 | | |
| 10 | | |

**Bonus. (4 points)**

Find, when the inputs enable (EN) is ON of Tri-State Buffer and Latch?
What does the following system do?
Hint: 3:8 Decoder is enable when E1=E2=0 and E3=1.
3:8 Decoder is an active low, example O1=0 when A2=A1=A0=0; and O3=O2=O1=1
IOW: Input/Output Write
IOW: Input/Output Read