NDU
Computer Architecture
CSC 312 Midterm.
Duration 1 hour 30 minutes.

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Name: [redacted]

1. The content of *PC* in the basic computer is **2F9** (all numbers are in hexadecimal). The content of *AC* is **AAAA**. The content of memory at address **2F9** is **D520**. The content of memory at address **520** is **3456**. The content of memory at address **345** is **FFFF**. The content of memory at address **456** is **EEEE**. Give the contents of the registers *PC, AR, DR, AC, IR, SC, E, & I* in hexadecimal at the end of the instruction cycle. (20 pts)

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PC = 2F9
AC = AAAA
M[2F9] = D520
M[520] = 3456
M[345] = FFFF
M[456] = EEEE

T_0 AR ← PC AR = PC = 2F9

T_1 IR ← M[AR], PC ← PC+1

PC = 2FA
IR = M[2F9] = D520

T_2 D 5 2 0

AR ← IR(0-11), I ← IR(15), IR(12->14) I = 1

AR = 520

When I decode I get 5 So my operation is ALA

T_3 since my I = 1 AR ← M[AR]

AR = 3456
AR = 456
Since AR = 1
12 4 7

T_4 M[AR] ← PC, AR ← AR+1

M[AR] = 25A
AR = 457

T_5 PC ← AR, SC ← 0

PC = AR = 457

PC = 521 457 DR = No change IR = D520 E = 0
AR = 521 AC = No change SC = 5 I = 1

2. In an 8-bit registers R1 & R2, starting from an initial value of R1 = 00110110, R2 = 01000111, what will be the value of R1 after each operation. (Use the new value of R1 for each new operation). (10 pts)

	Operation	Value of R1
a)	R1 ← Shl R1	01101100
b)	R1 ← R1v R2	01101111
c)	R1 ← Ashr R1	00110111
d)	R1 ← R1 + R2	01111110
e)	R1 ← Cil R2	10001110

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a) R1 00 11 0110
ShLR1 01 10 1100 → new R1

b) R1v R2 R_1 01101100
v R_2 01000111
01101111 → new R1

c) R1: 01101111
AshrR1 00110111 → new R1

d) R_1 00110111
+ R_2 + 01000111
01111110 → new R1

e) R_2: 01000111
CiLR2 10001110 → new R1.

3. Write the minimum sequence of micro-operations for the following instruction:

a. AC ← TR – IR – DR – 2 (10 pts)

AC ← TR - (IR + DR + 2)

AC ← 0

DR ← IR

AC ← IR

AC ← DR

DR

DR ← DR + 1

DR ← DR + 1

// DR + 2

AC ← DR , DR ← IR

AC = DR + 1
DR = IR

AC ← AC + DR , DR ← TR

AC ← $\overline{AC}$

AC ← AC + 1

AC ← DR + AC

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3. Write the minimum sequence of micro-operations for the following instruction:
   a. AC ← TR – IR – DR – 2 (10 pts)

AC ← TR - (IR + DR + 2)

~~AC ← 0~~

~~DR ← IR~~

~~IR AC ← DR~~ ~~DR~~

DR ← DR + 1

DR ← DR + 1

AC ← DR , DR ← IR

AC ← AC + DR , DR ← TR

AC ← $\overline{AC}$

AC ← AC + 1

AC ← DR + AC

// DR + 2

AC = DR + 2

DR = IR

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4. Using the common bus, check if each of the following instructions can be executed in one clock cycle; if yes, what will be the control signals to execute it, if not, say why? (10 pts)
   a. M[AR] ← DR, AC ← DR, IR ← 0
   b. PC ← M[AR], AC ← AC + DR, PC ← 0
   c. IR ← IR + 1, OUTR ← M[AR]

a) Yes
$S_2 S_1 S_0$ 011 write WR = 1 RD = 1 ALU(TRANSFER) = 1 LD(AC) = 1 CLEAR (IR) = 1

b) Yes $S_2 S_1 S_0$ 111 RD = 1 LD(PC) = 1 ALU(ADD) = 1 LD(AC) = 1 clear (PC) = 1 (PC ← 0, AC ← M(AR))

c) No since IR can just load we can not Increment

5. The memory unit of the basic computer is to be changed to a 65536 x 16 memory, requiring an address of 16 bits. The instruction format of a memory-reference instruction remains the same for I = 1 (indirect address) with the address part of the instruction residing in positions 0 through 11. But when I = 0 (direct address), the address of the instruction is given by the 16 bits in the next word following the instruction. Modify the micro-operations during time T_2, T_3, (and T_4 if necessary) to conform to this configuration. (10 pts)

2^{16}, 16 n = 16 k = 16

T_0 AR ← PC

T_1 IR ← M[AR], PC ← PC + 1

T_2 ~~AR ← IR(0, 11)~~ PC ← IR(0,16) I ← IR(15)

T_3 If I = 0 → AR ← PC; If I = 1 → AR ← IR(0,11)

T_4 AR ← M[AR] when I = 1

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6. Write an assembly program to count the positive values, the negative values, and the zero values in a block of memory starting at address 190, ending at address 200. (20 pts)

```
ORG 100
LDA PTR
CMA
INC
ADD EXP
INC
CMA
INR
STA CON
LOP, LDA PTR I
SPA
SZA
BUN JOA
ISZ ZER
BUN MEE
JOA, SPA
BUN LAR
ISZ POS
BUN MEE
END
LAR, ISZ NEG
MEE, ISZ PTR
ISZ CON
BUN LOP
HLT
PTR, HEX 190
EXP, HEX 200
CON, DEC 0
ANS, DEC 0
POS, DEC 0
NEG, DEC 0
ZER, DEC 0
END
```

6. Write an assembly program to count the positive values, the negative values, and the zero values in a block of memory starting at address 190, ending at address 200. (20 pts)

```
ORG 100
LDA PTR
CMA
INC
ADD EXP
INC
CMA
INR
STA CON
LOP, LDA PTR I
     SPA
     SZA
     BUN JOA
     ISZ ZER
     BUN MEE
JOA, SPA
     BUN LAR
     ISZ POS
     BUN MEE
LAR, ISZ NEG
MEE, ISZ PTR
     ISZ CON
     BUN LOP
     HLT
PTR, HEX 190
EXP, HEX 200
CON, DEC 0
POS, DEC 0
NEG, DEC 0
ZER, DEC 0
END
```

7. **Write an assembly program to divide a memory block, starting at address 150 and ending at address 200, into two memory blocks BlockA & BlockB (not necessary of the same size), where BlockA holds the odd operands, and BlockB holds the even operands. Find the ending address for each block if BlockA starts at address 201 and BlockB at address 301.** **(20 pts)**

```
ORG 100
LDA PTR
CMA
INC
ADD EXP
SNE
CMA
INC
STA CON
REG, LDA PTR I
CLE
CIR
SZE
BUN ODD
BUN EVE
ODD, LDA PTR I
STA BLA I
ISZ BLA
ISZ COA
BUN FIN
EVE, LDA PTR I
STA BLB I
ISZ BLB
ISZ COB
FIN, ISZ PTR
ISZ CON
BUN BLG
HLT
PTR, HEX 150
EXP, HEX 200
CON, DEC 0
BLA, HEX 201
BLB, HEX 301
```

operand is at location 100, and the last operand is at location 1??.

130 - 100

ORG 250
LDA PTR I
CMA
INC
ADD EXP
INC
CMA
INC
STA CON

HLT
PTR, HEX 100
EXP, HEX 150
CON, DEC 0
ANS, DEC 0
NUM, DEC 4

~~HEE, LDA PTR I~~

To divide by 4
I have to SHR twice

FIN, ISZ PTR
ISZ CON
BUN HER
HLT

HER, LDA NUM
CMA
INC
ADD PTR I
SZA
BUN HLA
BUN ZER

HLA SNA
BUN HER
BUN FIN
ZER ISZ HER

G☺☺D Luck

Explain to me in Class ??

I did long !

8. Extra Problem: (10 pts)
Write an assembly program to count the number of operands that can be divided by (4), The first operand is at location 100, and the last operand is at location 150.

```
ORG 250
LDA PTR I
CMA
INC
ADD EXP
SNE
CMA
INC
STA CON
HER, LDA PTR I
     ISZ PTR
     ISZ CON
     BUN HER
     HLT
FIN, ISZ PTR
     ISZ CON
     BUN HER
     HLT
```

```
HLT
PTR, HEX 100
EXP, HEX 150
CON, DEC 0
ANS, DEC 0
NUM, DEC 4
HER, LDA NUM.
     CMA
     SNE
     ADD PTR I
     STA PTR I
     SZA
     BUN HER
     SNA
     BUN HER
     ISZ HER
     BUN HLA
     BUN ZER
HLA  SNA
     BUN HER
     BUN FIN
ZER  ISZ HER
```

To divide by 4
I have to shr twice

Explain to me in Class ??

GOOD Luck

I did long !