

# Notre Dame University

### ECCE Department

Exam #1

Spring Semester (2004-2005)

## **Microprocessor Design Systems** EEN324

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Student ID: \_\_\_\_\_Solution

Question1 Question2 Question3 Question4 Total

10
25
10
15
/60

#### **<u>Question 1.</u>** (10 points)

Answer True or False for each of the following statements (1 point each)

1. An instruction that has 2 machine cycles would require 2 clock cycles to complete	Т	F
2. All registers in the 8085 are 8-bits	Т	F
3. Memory stores information in Hexadecimal format.	Т	F
4. The microprocessor (8085) is made up of a Control Unit, an Arithmetic and Logic Unit, and Registers.	Т	F
5. Only one device can be connected to a unidirectional bus.	Т	F
6. It is possible to have F130H as the first address of a 1K memory chip.	Т	F
7. An 8-bit microprocessor (8085) has 8 address lines.	Т	F
8. A register is very fast memory located inside the microprocessor.	Т	F
9. A 2 Mega Byte memory chip has 21 address lines and 8 data lines.	Т	F
10. ALL Arithmetic and Logic operations in the 8085 use the accumulator.	Т	F
11. The Operating System is the first program to execute after startup and the last program to quit.	Т	F

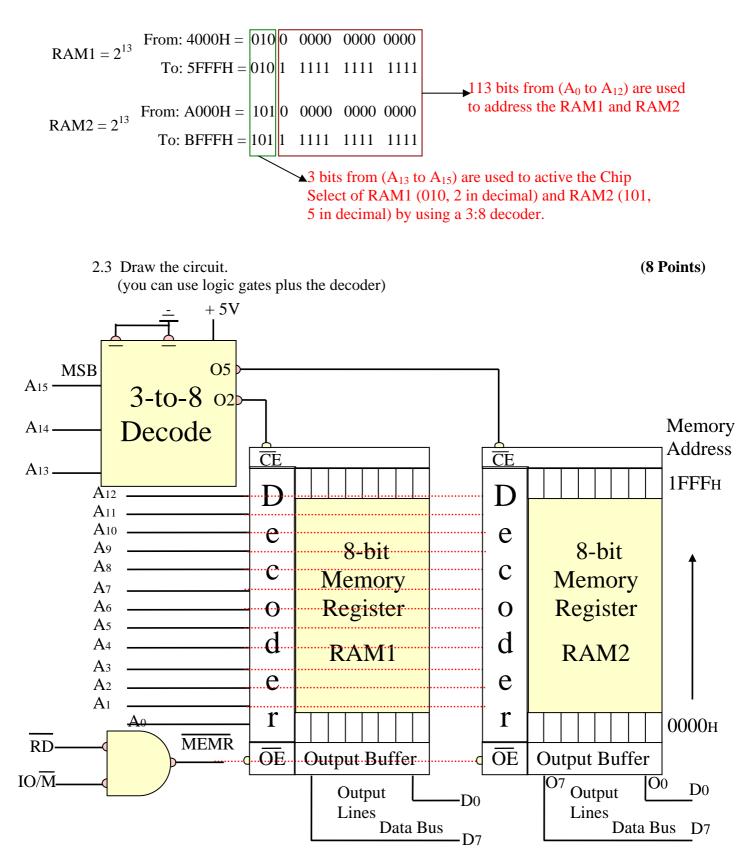
#### **<u>Question 2</u>**. (25 points)

An existing memory system has the memory map shown in Figure 1.

	т0000H
16 K RAM1	3FFFH 4000H
New RAM chip1	5FFFH
8 K RAM2	6000H
8 K RAM3	7FFFH 8000H
	9FFFH A000H
New RAM chip2	BFFFH
16 K EPROM	С000Н
FIGURE 1	FFFFH

2.1 Determine the starting and ending addresses for each of the new memory chips. (10 Points)

RAM1 =  $2^{13}$  = 8K From: 4000H To: 5FFFH RAM2 =  $2^{13}$  = 8K From: A000H To: BFFFH 2.2 Determine the combinations needed for the chip select of the new memory chips. (7 Points)



#### **<u>Question 3</u>**. (15 points)

Using the following timing diagram, find the instructions executed by the 8085 microprocessor.

And what is the address at the M6 machine cycle?

Refer to the following table to find the instructions, **not all are used**.

		Μ	<b>I</b> 1			M2		•••••	Ν	13			M4			M5			M6	
	T1	T2	Т3	T4	T1	T2	T3	T1	T2	Т3	T4	T1	T2	T3	T1	T2	T3	T1	T2	T3
A7 A0		00H		Unspe cified	Y		00H				Unspe cified			00H					??H	
AD7 AD0	60H	- 3E	н	<b>-</b>	61H	[	32H	62H	- 32	2н	<b>-</b>	63H	<b>-</b> [ (	юн	64H	- 80	H -	00H	- 32	┨ ┣.
ALE													J L						J <b>L</b>	
IO/M																				
RD																				
WR MEMW																				

	Hex. OpCode	Mnemonics	#T-States
MVI A, 32 STA 8000	00	NOP	4
STA 0000	32	STA	13
	3E	MVI A,	7
	60	MOV H,B	4
	61	MOV H,C	4
	62	MOV H,D	4
	63	MOV H,E	4
	64	MOV H,H	4
	80	ADD B	4

Count

#### **<u>Question 4</u>**. (15 points)

Design an I/O system for the 8085 microprocessor with the following characteristics:

- An input peripheral-mapped port with address 42H.
- An output memory-mapped port with address 4x3xH (x means don't care).

Assume that the device selection input for both ports is active low.

You are limited to the following chips (Max):

Chip type

	Chip type	Count
	3:8 Decoder	1
	Octal Latch gate	1
	Octal D-Flip-Flop	1
	4-inputs NAND gate	5
	4-inputs OR gate	3
	Inverter gate	6
A0 A1 A2 A3 A15 A14 A13 A12 A7 A4 A1 A14 A13 A12 A7 A7 A7 A14 A14 A13 A12 A7 A7 A7 A7 A7 A7 A7 A7 A7 A7 A7 A7 A7	Inverter gate $D \leftarrow 74LS244$ $a \leftarrow Octal$ $B \leftarrow U \leftarrow B$ $U \leftarrow B \leftarrow OE$ OE OE OE $D7 \leftarrow D \leftarrow D \leftarrow D$ $a \leftarrow a$ t = a $D7 \leftarrow D \leftarrow$	6 D a t a I N D a t a t a
	$\begin{array}{c c} B \\ u \\ D_0 \end{array} \begin{array}{c} 74LS373 \\ Octal \\ D-Latch \end{array}$	O U T
Input PORT address 42: xxxx xxxx Output Memory address 4x3x: 0100 xxxx		

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