H.U. Spring 2010

Name: ----------

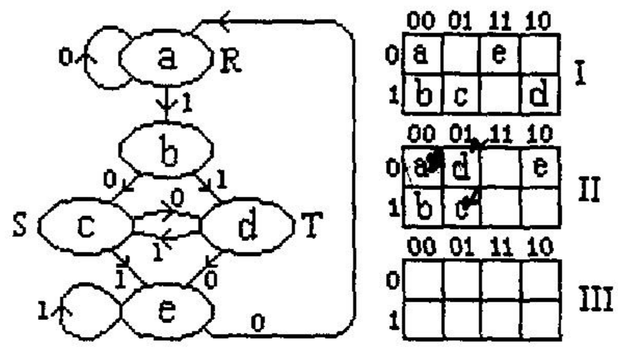
PHY 233
Quiz II

1. In the state transition diagram R, S, and T are outputs.

   a. What are the priorities (rules) in the state assignment maps I ? *(8 pts.)*

   b. What are the priorities (rules) in the state assignment maps II ? *(6 pts.)*

   Bonus: *Can you suggest an assignment (III) that avoids the violations in I & II? Justify your answer briefly*

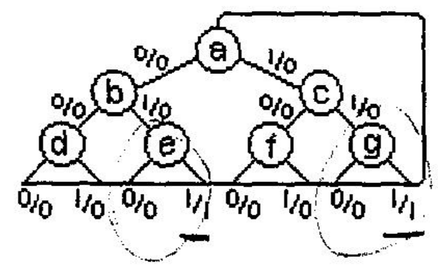


---

2. For the state transition diagram shown

   a. Reduce the number of states by the method of grouping. *(12 pts.)*

   b. Draw the reduced state transition diagram. *(5 pts.)*



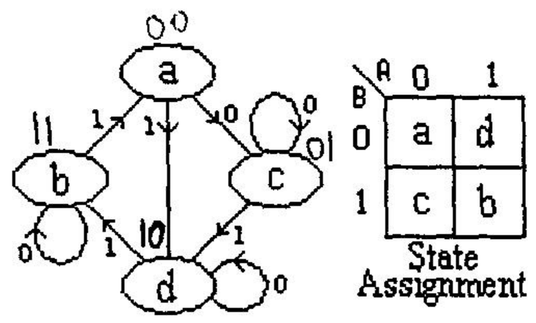
---

3. The figure shows a flow chart and its state assignment. The input is (x)

   a. Prepare the present state-next state charts *(3 pts.)*

   b. Prepare the Karnaugh Maps for D_A and D_B *(6 pts.)*

   c. Convert the D_B map to JK maps *(6 pts.)*



---

4. Realize the circuit of Q3 by D Flip Flops and Mux implementation.
   You will be graded on the basis of consistency with your answer for part (b) *(10 pts.)*

---

5. Answer 5 of the following 8 questions briefly: *(6x5 = 30 pts.)*

   a. How many 16x4Bit memory chips (our own 74189) are needed to construct a 1Kbyte memory ?

   b. How do registers help to remove glitches at the output?

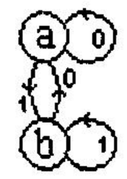
   c. What is the advantage in using a One-Hot state Machine? What is the price paid?

   d. What are the disadvantages of Mux realizations of ASM's?\

   e. What is(are) the advantage(s) of state reduction?

   f. Why isn't any Johnson counter self correcting?

   g. How many distinct state assignments will there be if we use a 2-bit address for the ASM shown? Justify your answer explicitly showing the state assignment map(s)



Good Luck!

14 + 17 + 15 + 10 + 30 = 100