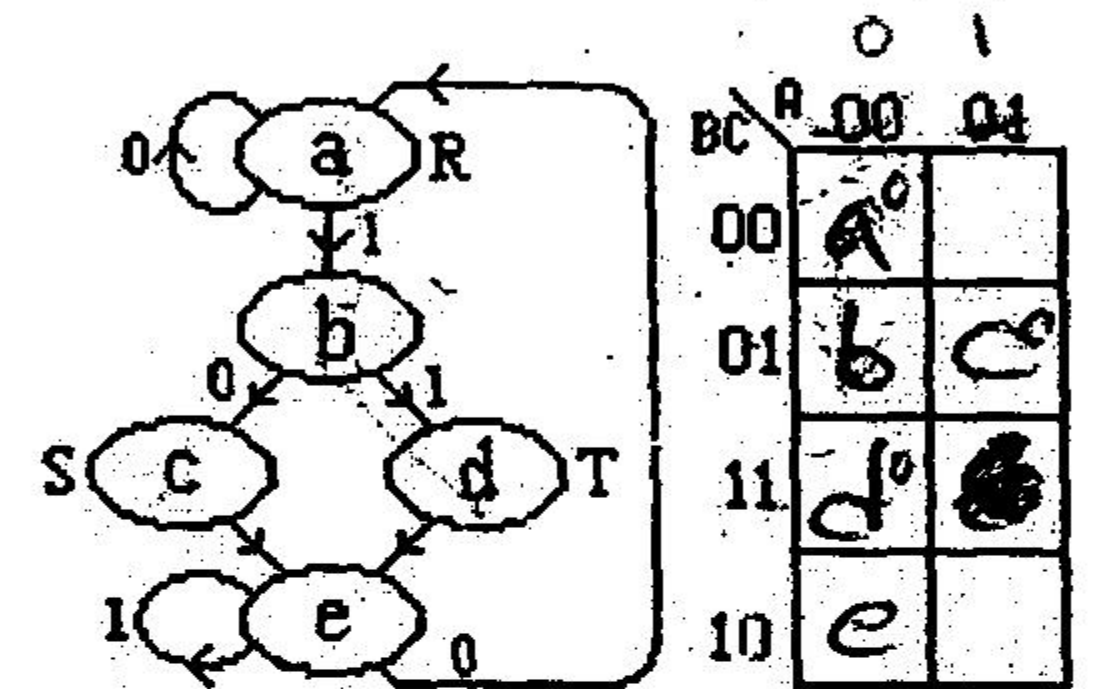


PHY 233
Quiz II

1. a. Realize the state assignment for the state transition diagram (which has outputs R, S, and T.) such as to avoid output glitches.
(No points for other considerations. You may save time by answering on the blank map next to the diagram) (15 pts.)

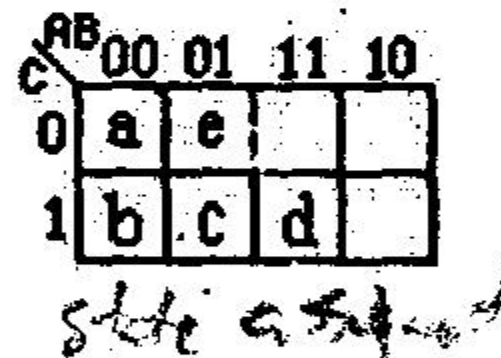


8x7x6x5x4
2³ x 3! ←

- b. Calculate the number of DISTINCT state assignments. (5 pts.)

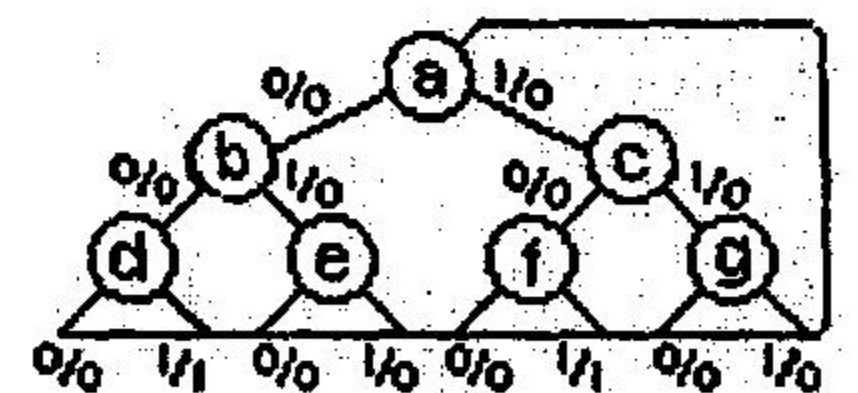
2. Assume that the state assignment shown is made for the state transition diagram of question 2 above.

- a. Prepare the Karnaugh maps for D_A, D_B, and D_C (12 pts.)
b. Convert (only) the D_B map to J_B and K_B, and calculate them. (8 pts.)

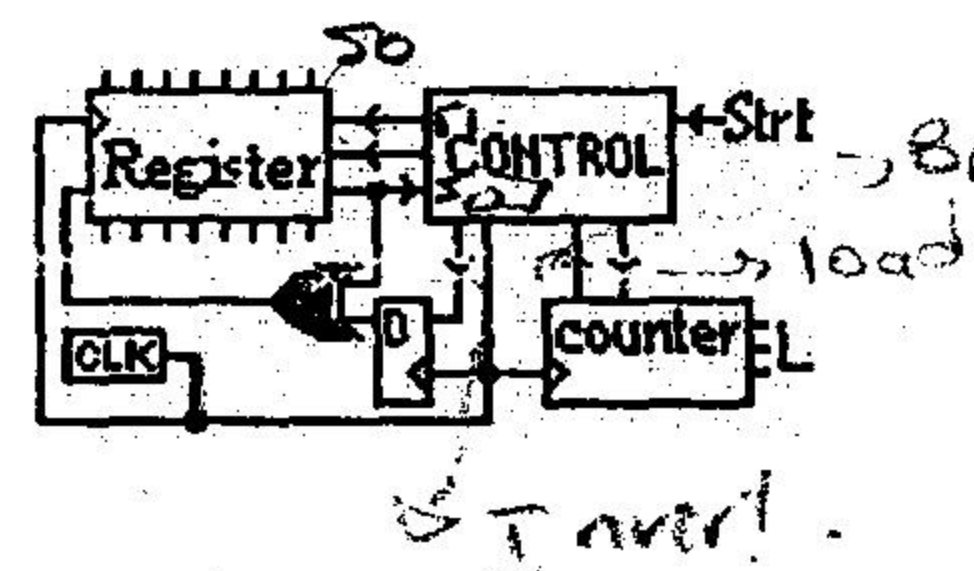


3. The For the state transition diagram shown

- a. Reduce the number of states by the method of grouping (12 pts.)
b. Draw the reduced state transition diagram. (3 pts.)

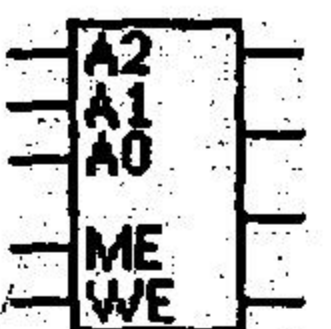


4. a. Identify the computation performed by the circuit. 2's complement (4 pts.)
b. Label the 6 arrowed wires that go in/out of the control. (12 pts.)
(No points for Start and Clock)



5. The figure shows a memory chip. A stands for Address, ME and WE stand for Memory Enable and Write Enable. NXM Memory = N words of length M

- a. How many such chips would you need to construct a 16x16 memory? (5 pts.)
b. Show how one construct a 16X8 memory using this chip. (10 pts.)



6. Answer 3 of the following 4 questions. (3x5 = 15 pts.)

Note: The 4th answer will be ignored.

- a. Define "reduced input dependency" logically adjacent to the correspond to binary variable.
b. Why is clock suppression used? for carry propagation delay to finish "for product" 2b synchron
c. Why are analogue inputs multiplexed into a single ADC?
d. What are the disadvantages of Mux realizations of ASM's? Many space, slow "Mux gates" here

Good Luck!

1101010
0010110
4) a) The control loads the 7100 by the number to be complement, IT shifts the no, from S0 to S1 till the 1st one arrives after which A the 7100 complement will be set.
2x20 + 16 + 3x15 = 101