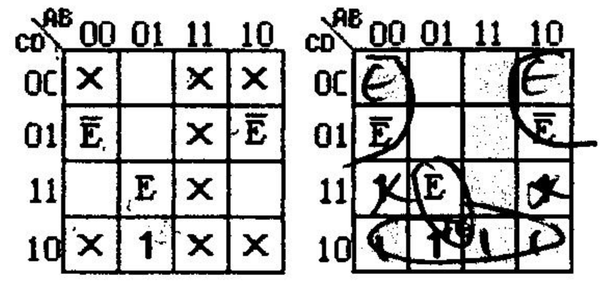
H.U. Spring 2009
Dr. H. Barsoumian

Name: ----------

PHY 233
Quiz I.



1. Replace the "Don't Cares" with appropriate values, and write down a minimized logic function for the map shown. Fill in the values of the X's explicitly in the blank map. *(Correctness: 13 pts. Minimalism: 5 pts.)*

---

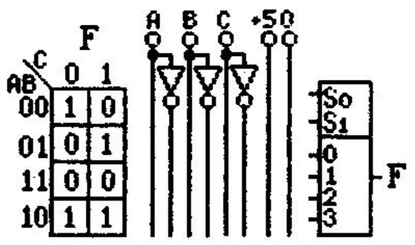
2. Follow the Quine-McCluskey method to minimize $F = m_0 + m_6 + m_7 + m_9 + m_{11} + m_{13} + m_{15}$
   Note: You must show ALL your steps and reasoning explicitly. *(21 pts.)*

	m_0	m_6	m_7	m_9	m_{11}	m_{13}	m_{15}

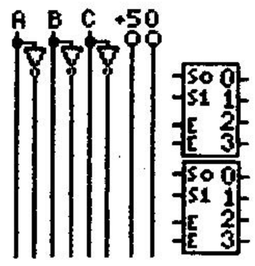
---

3. Answer one of the following two problems: *(18 pts.)*

3A. Show how the function (F) defined by the map can be realized using the Mux given.
You will save time by using the diagram itself.

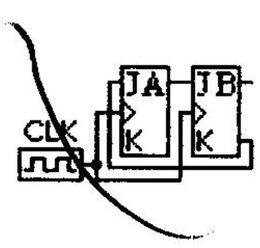


3B. Show how the two decoders should be connected to obtain a 3:8 decoder. S_0 & S_1 are the addresses, whereas the E's stand for enable.

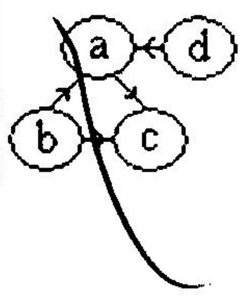


---

4. Fill the table with the appropriate values of J_A, K_A, J_B, and K_B. Calculate the next values A_{n+1}, B_{n+1}, Show that it is a self correcting MOD3 counter. Identify the states a, b, c, and d in the diagram *(18 pts.)*



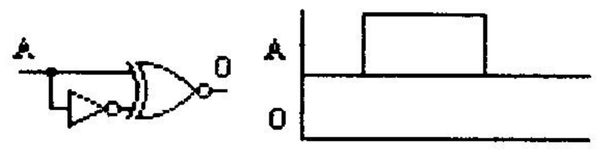
A_n B_n	J_A K_A	J_B K_B	A_{n+1} B_{n+1}
0 0			
0 1			
1 0			
1 1			



---

5. Answer 5 of the following 7 questions briefly. The 6th answer will be ignored. *(5x5 = 25 pts.)*

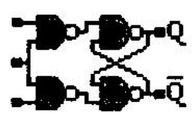
a. Draw the output of the circuit shown assuming that the delay is one division. Mention a possible use.



b. Give a possible advantage of having more than one enable pin in a chip.

c. What are the advantages of minimizing logic functions?

d. Identify the circuit shown and label the three inputs.



e. Perform the Binary division 10101/11 EXPLICITLY. (*No points for answers like 45/5 = 9*)

f. Why do we always see a 3-bit OR gate at the inputs of each flip-flop in a shift register?

g. How does the Gray code differ from the regular sequence of digital numbers? Explain with the aid of a diagram.

Good Luck!

3x18 + 21 + 25 = 100