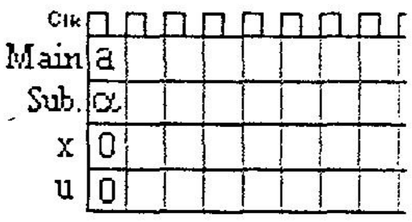
H.U. Spring 2010

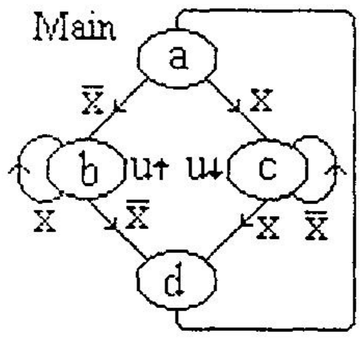
Name: ----------

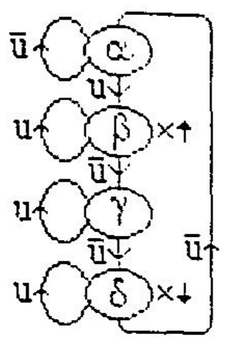
PHY 233
Final

Note: You may save time by answering parts of Q's: 1, 2, 3, 4, 5 on the question sheet itself.

1. The figure shows two sequences and the beginning of a timing diagram. The first coloumn shows the initial state of the two systems. Continue the diagram for at least 8 cycles of the clock.
Do you observe a vicious cycle? *(10 pts.)*







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2. The figure shows a simple Asynchronous State machine, a State Transition Diagram, and two maps (M1 and M2).

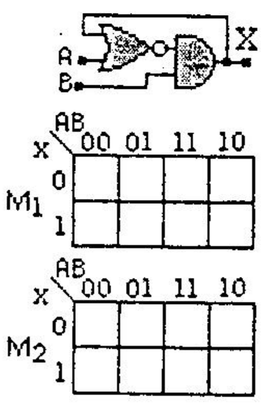
a. Calculate (X) and record it in the map M_1. *(2 pts.)*

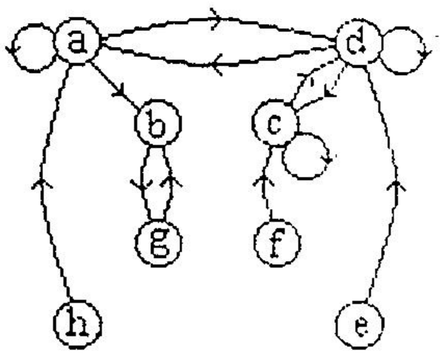
b. Identify the stable states on the map M_1. *(3 pts.)*

c. Show the state assignment (a to g) on M_2 *(4 pts.)*

d. Show (AB) on the arrows wherever appropriate *(3 pts.)*

e. Can there be racing? Can this ASM be used? *(3 pts.)*





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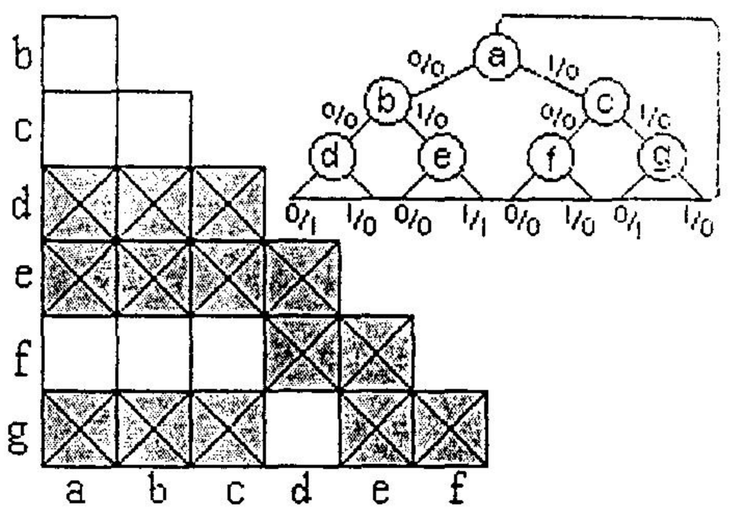
3. The figure shows a state transition diagram and a partially filled Implication chart.

a. Explain why are 14 of the 21 cells crossed out? *(2 pts.)*

b. Fill the blank cells and identify the redundant state(s) *(5 pts.)*

c. Redraw the minimized state diagram *(3 pts.)*

d. State the operation performed by the ASM. *(2 pts.)*



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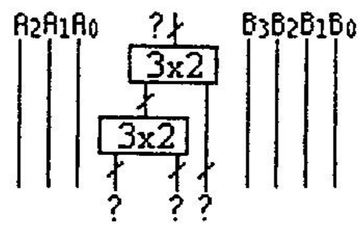
4. The figure shows two 3x2 Multiplication blocks used to construct a 3x4 block.

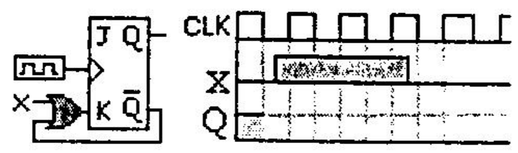
a. Show how the inputs are connected to the multiplication blocks *(4 pts.)*

b. Indicate the number of bits on each slash sign marked by (?) *(3 pts.)*

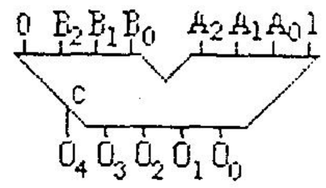
c. Draw the details of the 3x2 block. Do NOT forget to include the correct carry in. Yes, you should have done the HW. *(5 pts.)*



At t = 0 we have Q =1. Continue the timing diagram for 5 cycles.
Note that the input J is not connected. *(8 pts.)*

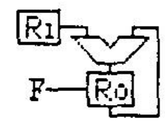


Answer 8 of the following 13 questions.
The 9th answer will be ignored. *(8x5.5 = 44 pts.)*



a. Evaluate the output of the adder in terms of A&B.
Why is the C pin added to the output?

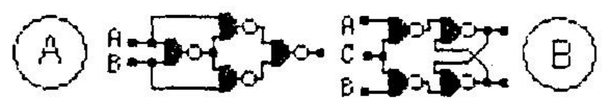
b. Why is the power dissipated in a chip proportional to its speed?



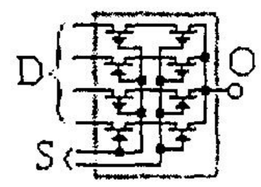
c. Write a Register Transfer Language statement for the Adder circuit shown.

d. In which situation would one use an SAR and rather than a Continuous ADC?

e. Identify the two gates that the NAND chip is simulating in the figure.

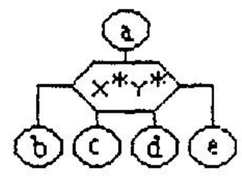


f. Why is serial asynchronous data preceded by a "1"?



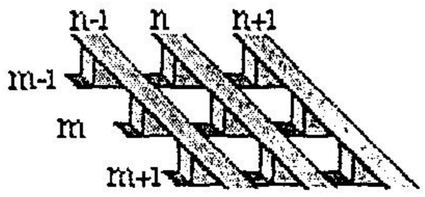
g. Identify the chip constructed of Transmission gates.

h. When is an Associative Memory useful?



i. Why is the branching shown on x*y* unwise?

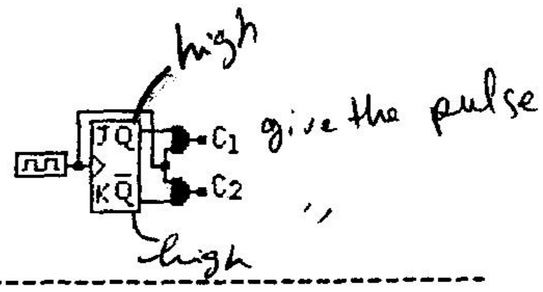
j. In sequential computation, why can loading the length of the numbers be optional?



k. Identify the segment that looks like 3 highway lanes.
What do the indices m & n refer to?

l. What is the algorithm of the Boozer ?
No points for saying: Find booze, drink booze…

m. Identify the circuit shown. Why is it essentially an ASM?



Good Luck! *10+15+2x12+8+44 = 101*

Bonus: *What would be the greatest practical difficulty in constructing an ASM by Logic Works?*